A 40 MHz IF Fourth-Order Double-Sampled SC Bandpass ΣΔ Modulator

Seyfi Bazarjani and Martin Snelgrove
Department of Electronics, Carleton University, Ottawa, Ontario, Canada K1S-5B6
E-mail: seyfi@doe.carleton.ca

Abstract: A fully differential double-sampled SC architecture for a fourth-order bandpass ΣΔ modulator is presented. This architecture is based on a double-sampled SC delay circuit. The effect of opamp DC gain on the notch frequency of this modulator is analyzed. The modulator is implemented in a 0.5 μm CMOS technology and operates at a clock frequency of 80 MHz. Thus, the effective sampling rate is 160 MHz. The image signal is about 40 dB below the fundamental signal. Over a 2 MHz bandwidth centered at 40 MHz, the measured SNDR is 45 dB (not including the image). The circuit operates at 3.3 V and consumes 65 mW.

1.0 Introduction

High-speed bandpass ΣΔ modulators are desired in applications that require A/D conversion of narrow-band signals at IF frequencies such as high-speed modems and digital radios. Increasing the sampling frequency of a bandpass ΣΔ modulator allows A/D conversion of the signal at higher IF frequencies. Digitizing the analog signal at a high IF and processing the signal in the digital domain is desirable due to the robustness of the digital circuits.

Switched Capacitor (SC) is the preferred analog technique for the implementation of ΣΔ modulators due to its high circuit accuracy. The operating speed of an SC circuit is determined by the settling time of the opamp used in the circuit. A method of increasing the sampling frequency is to use the opamp during both phases of a clock [1] i.e., double-sampling. This technique increases the sampling frequency by a factor of two without requiring a faster opamp. Double-sampling has already been applied to design lowpass ΣΔ modulators [2][3]. Here, a novel double-sampled SC fourth-order bandpass ΣΔ modulator is presented. The impact of low opamp DC gain on the performance of this modulator is analyzed. The modulator was designed and fabricated in a 3 V 0.5 μm CMOS technology to verify its performance and functionality.

2.0 Double-Sampled SC Bandpass ΣΔ Modulator

The z-domain architecture of a fourth-order bandpass ΣΔ modulator is shown in Fig. 1. This structure is a direct map of the lowpass ΣΔ modulator in [4] to bandpass by transforming integrators to resonators. This

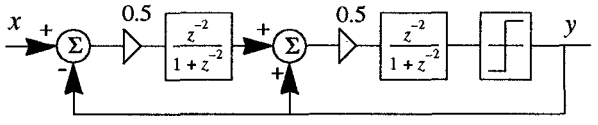

Fig. 1: A fourth-order bandpass ΣΔ modulator

transformation maps zeros of the lowpass prototype from DC to $\pm f_s/4$. Therefore, noise in the resulting bandpass modulator is suppressed around the $f_s/4$ frequency.

The $f_s/4$ resonator can be implemented in several different ways using SC techniques. In [5], resonators are implemented using Lossless Discrete Integrators (LDI) and Forward-Euler (FE) integrators. Another approach is to use two delay cells in a negative feedback loop [6], as shown in Fig. 2.

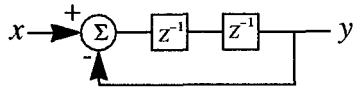

Fig. 2: Resonator using delay cells

An efficient architecture for a unity gain SC delay circuit which is immune to capacitor mismatch is presented in Fig. 3.

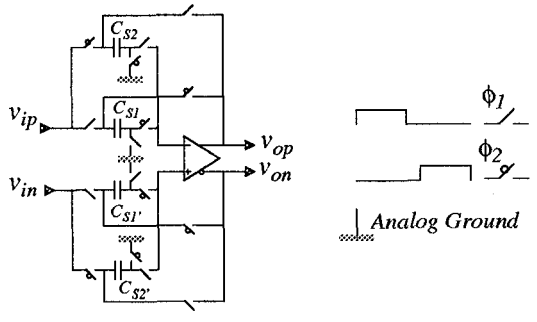

Fig. 3: A double-sampled SC delay circuit and its clock phases

In this circuit, the input signal is sampled every half clock period ($T_s/2$) and appears at the output with a half-clock period delay. Thus, the transfer function of this cell is

$$V_{od}(\hat{z})/V_{id}(\hat{z}) = H_{iD}(\hat{z}) = \hat{z}^{-1}, \qquad (1)$$

where $\hat{z} = e^{j\omega(T_s/2)}$.

Therefore, the effective sampling frequency in this two-path sample-and-hold circuit is twice the clock

frequency. The factor-of-two improvement in the speed of the double-sampled SC delay cell is achieved without increasing the clock rate or requiring a faster opamp settling time. In return, mismatch and uneven clock phases create image errors as is discussed in [7].

Finite opamp gain (A) and non-zero opamp input capacitance (C_{in}) cause error in the ideal transfer function of the double-sampled SC delay circuit and the actual transfer function is given by [7]

$$\frac{V_{od}(z)}{V_{id}(z)} = H_{aD}(z) = \left[\frac{g_0}{1-p_0 z^{-1}}\right] z^{-1} \qquad (2)$$

where g_0 and p_0 are given by

$$g_0 = \frac{1}{1+\frac{1}{A}+\frac{C_{in}}{C_S}\cdot\frac{1}{A}} \qquad p_0 = \frac{C_{in}}{C_S}\cdot\frac{g_0}{A}. \qquad (3)$$

Thus, finite opamp gain and non-zero input capacitance modify the transfer function of the double-sampled delay cell by a damped integrator term from its ideal response. This change of transfer function causes both gain and phase error in the response of the delay circuit. The actual transfer function becomes

$$H_{aD}(z) = \left[m_{aD} e^{j\theta_{aD}}\right] \cdot z^{-1}, \qquad (4)$$

where m_{aD} and θ_{aD} are the magnitude and phase of the error term in the double-sampled delay circuit. Assuming $A \gg 1$, the magnitude and phase error are given by

$$m_{aD} \approx 1 - \frac{1}{A\beta} + \frac{\cos\omega T}{A}\left(\frac{C_{in}}{C_S}\right) \qquad (5)$$

$$\theta_{aD} \approx -\frac{\sin\omega T}{A}\left(\frac{C_{in}}{C_S}\right). \qquad (6)$$

A double-sampled SC resonator is obtained by cascading two double-sampled delay circuits as shown in Fig. 4. The ideal transfer function of this circuit is

$$H_{iR}(z) = \frac{C_I}{C_{S1}} \cdot \frac{z^{-2}}{1+z^{-2}}. \qquad (7)$$

As was shown above, finite opamp gain (A) causes errors in the ideal transfer function of a double-sampled SC delay circuit (given by (4)) and the actual transfer function of a double-sampled resonator becomes

$$H_{aR}(z) = \frac{C_I}{C_{S1}} \frac{\left[\left(m_{aD1} e^{j\theta_{aD1}}\right)\left(m_{aD2} e^{j\theta_{aD2}}\right)\right] z^{-2}}{1+\left[\left(m_{aD1} e^{j\theta_{aD1}}\right)\left(m_{aD2} e^{j\theta_{aD2}}\right)\right] z^{-2}}. \qquad (8)$$

Poles of this resonator are

$$z_{p1,p2} = \pm j\sqrt{m_{aD1}\cdot m_{aD2}}\cdot e^{j\frac{(\theta_{aD1}+\theta_{aD2})}{2}}. \qquad (9)$$

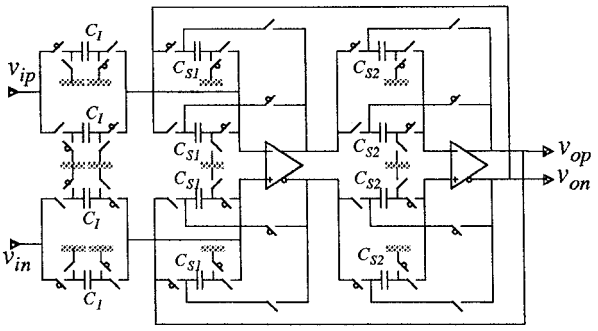

Fig. 4: A double-sampled SC resonator

The poles are inside the unit circle, close to the intersection of $j\omega$-axis and the unit circle. The phase error of the poles of this resonator in radians is

$$\theta_{aR} = -\frac{\sin\omega T}{2A}\left[\frac{C_{in1}}{C_{S1}} + \frac{C_{in2}}{C_{S2}}\right]. \qquad (10)$$

Both magnitude and phase errors are inversely proportional to the DC gain of the opamp.

A double-sampled double-resonator SC bandpass ΣΔ modulator is constructed using two double-sampled resonators and a quantizer in a feedback loop, as shown in Fig. 5

All the capacitors are unit size capacitors C_u, except for the eight marked by asterisks which have a value of $2C_u$, and are made of two unit size capacitors in parallel. The gain of resonators is set by these eight capacitors to the required value of 0.5.

The functionality of this double-sampled SC bandpass ΣΔ modulator was verified in Eldo using near ideal components. The on-resistance of the switches was set to 200 Ω and the DC gain of opamps was assumed to be 60 dB. Fig. 6 shows the output spectrum of the modulator for a sinusoid input signal of 50.1 MHz. The amplitude of the signal was 12 dB below full scale and the clock frequency was 100 MHz. Simulated SNDR is 72.8 dB and 57.8 dB for bandwidths of 1 MHz and 2 MHz respectively.

Double-sampled SC circuits are sensitive to path mismatch and any mismatch between the two channels will produce image problems. Mismatch in the second stage of the modulator is noise shaped (second-order noise-shaping) and will not cause a noticeable image signal. However, mismatch in the first stage of the modulator is critical and must be avoided. A path mismatch of ±1 % on the input in the first stage of the modulator will produce an image signal which is only 40 dB below the signal. The above arguments were verified by simulations[7].

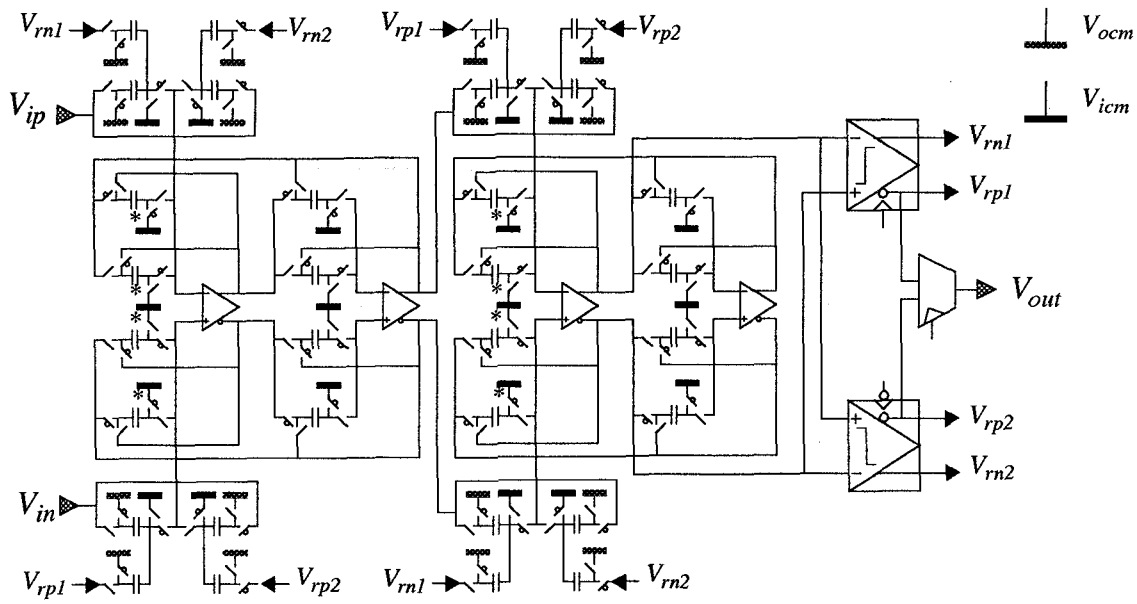

Fig. 5: A fourth-order double-sampled SC bandpass sigma-delta modular

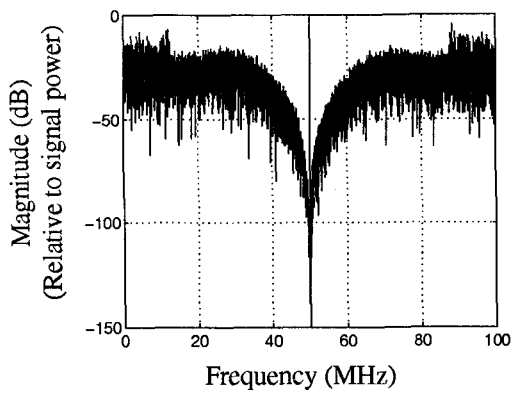

Fig. 6: Output spectrum from Eldo simulation

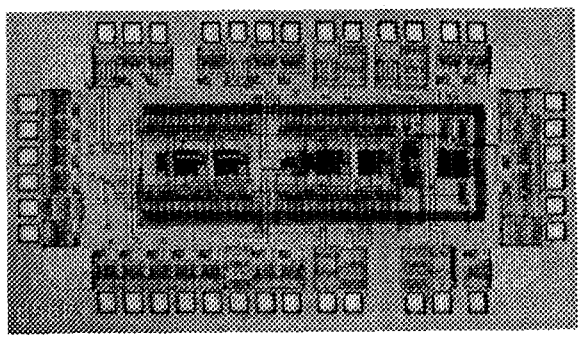

Fig. 7: Chip microphotograph of the fourth-order double-sampled SC bandpass ΣΔ modulator

3.0 Implementation

The fourth-order double-sampled SC bandpass ΣΔ modulators in Fig. 5 was designed and fabricated in a 0.5 μm double-poly CMOS process. Fig. 7 illustrates the chip microphotographs of the modulator. The active chip area of this circuit is about 1.1 mm^2.

The main objective of the design was to demonstrate high-speed SC capabilities in submicron CMOS technologies. In [5], it is shown that SC circuits operating at 40 MHz are feasible in a 0.8 μm BiCMOS process. Here, the target clock frequency was set to be 80 MHz—the effective sampling frequency was 160 MHz. Therefore the IF frequency was at 40 MHz.

To achieve high speed at moderate power, the unit capacitors are chosen to be small, 300 fF. The total in-band kT/C noise of this modulator is calculated to be less than −76 dB relative to 2 V_{PP} signal.

Switches are parallel nMOSFET and pMOSFET transistors with a worst case on-resistance of 333 Ω. This ensures the settling error to be less than 0.1 %.

A single stage cascode opamp (also called a telescopic opamp) is used to achieve the high speed and adequate DC gain needed for the opamp. The schematic of a fully differential cascode opamp designed to fulfill these requirements is shown in Fig. 8. A continuous time common-mode feedback circuit sets the output common mode to the desired value. Resistors in the common-mode feedback circuit have a high value of 68 kΩ to ensure the opamp DC gain does not drop below 54 dB. The capacitors in the common mode feedback circuit have a value of 400 fF. This opamp operates at 3.3 V, has a simulated DC gain of 54 dB, a unity gain bandwidth of 650 MHz, a phase margin of 70° when driving a 1 pF load, and consumes 8.8 mW.

Due to model inaccuracy of MOS output conductance, measured opamp DC gain was about 40 dB.

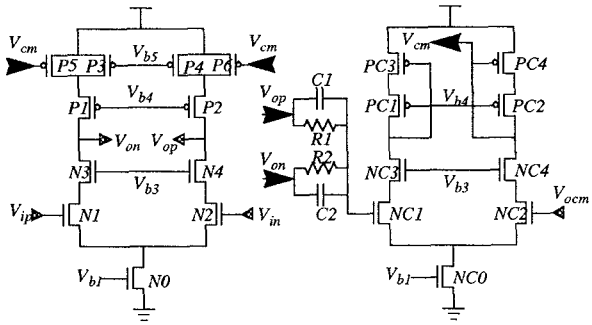

Fig. 8: Fully differential cascode opamp

4.0 Measurements

The double-sampled bandpass SC ΣΔ modulator was tested at 3 V and a clock frequency of 80 MHz and consumes 65 mW .Fig. 9 shows the output spectrum of the modulator for an input sinusoid at 40.8 MHz with an amplitude of 6 dB below full scale.

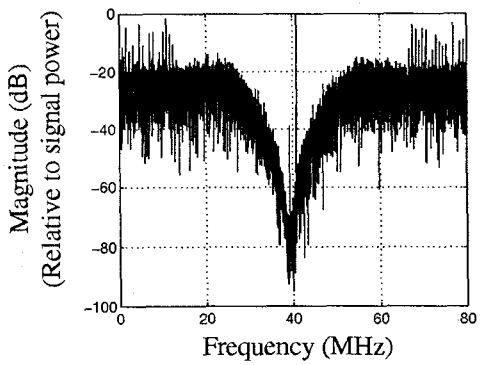

Fig. 9: Measured output spectrum of the fourth-order double-sampled SC bandpass ΣΔ modulator

The output bit-stream was captured by a logic analyzer for 16384 clock cycles. In Matlab, a 16384-point FFT was carried out to compute the output spectrum. The image signal is at 39.2 MHz and is 39 dB below the signal. This suggests that the capacitor mismatch is about 1 %. Using layout techniques such as common-centroid, good capacitor matching—in the order of 0.1 %—can be achieved. A capacitor mismatch of 0.1 % will reduce the power of image signal to about 60 dB below the signal power. This kind of accuracy is acceptable for some applications, such as cable modems and PCS basestations. DSP techniques can also be used to postprocess the data and cancel the image.

Measured SNDR of this modulator is about 47.3 dB and 45 dB for bandwidths of 1 MHz and 2 MHz respectively if the image is ignored.

Fig. 10 illustrates an expanded view of the output spectrum around 40 MHz. As we can observe, the notch frequency of the modulator is shifted to about 39 MHz, which is 1 MHz below the expected value of 40 MHz. This is due to low opamp DC gain. Using (6), the opamp DC gain is calculated to be 40 dB.

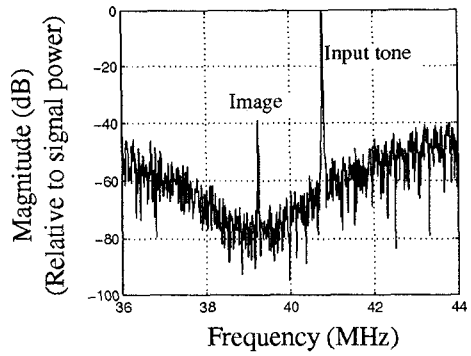

Fig. 10: Expanded view of the output spectrum around the notch

5.0 Conclusions

A new double-sampled SC bandpass ΣΔ modulator was presented. An analytical expression for the notch shift due to low opamp DC gain was derived. Design and measurement results in a 0.5 μm CMOS process were also presented.

Acknowledgments

The authors would like to acknowledge the financial support received from Nortel and from NSERC.

References

[1] T.C. Choi and R.W. Broderson, "Considerations for High-Frequency Switched-Capacitor Ladder Filters," *IEEE Trans. Circuits and Systems*, vol. CAS-27, no. 6, pp. 545-552, June 1980.

[2] P.J. Hurst and W.J. McIntyre, "Double Sampling in Switched-Capacitor Delta-Sigma A/D Converters," in *Proc. IEEE International Symposium on Circuits and Systems*, 1990, pp. 902-905.

[3] T. Burmas, S. Lewis, P. Hurst, and K. Dyer," A Second-Order Double-Sampled Delta-Sigma Modulator," in *Proc. CICC*, 1995. pp. 195-198.

[4] B. Boser and B. Wooley, "The design of sigma-delta modulation analog to digital converters," *IEEE JSSC*, vol. 23, pp. 1298-1308, Dec. 1988.

[5] Frank W. Singor and W.M. Snelgrove, "10.7MHz Bandpass Delta-Sigma A/D Modulators," in *Proc. CICC*, May 1994, pp.163-166.

[6] L. Longo and B. Horng, "A 15b 30kHz Bandpass Sigma-Delta Modulator," in *ISSCC Digest of Technical Papers*, Feb. 93, pp. 226-227.

[7] Seyfi Bazarjani, *Mixed Analog-Digital Design Considerations in Deep Submicron CMOS Technologies*, Ph.D. Thesis, Carleton University, Ottawa, July 1996.