

# Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators

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**Abstract**— The performance of continuous-time (CT) delta-sigma modulators ( $\Delta\Sigma$ 's) suffers more severely from time jitter in the quantizer clock than discrete-time designs. Clock jitter adds a random phase modulation to the modulator feedback signal, which whitens the quantization noise in the band of interest and hence degrades converter resolution. Even with a perfectly uniform sampling clock, a similar whitening can be caused by metastability in the quantizer: a real quantizer has finite regeneration gain, and thus, quantizer inputs near zero take longer to resolve. This paper quantifies the performance lost due to clock jitter in a practical integrated CT  $\Delta\Sigma$  clocked with an on-chip voltage-controlled oscillator. It also characterizes metastability in a practical integrated quantizer using the quantizer output zero-crossing time and rise time as a function of both quantizer input voltage and the slope of the input voltage at the sampling instant, and predicts the maximum-achievable performance of a practical CT  $\Delta\Sigma$  given jitter and metastability constraints.

**Index Terms**—Delta-sigma modulation, jitter, metastability.

## I. INTRODUCTION

**D**ELTA-SIGMA modulators ( $\Delta\Sigma$ 's) [1], [2], are popular nowadays for analog-to-digital conversion applications.  $\Delta\Sigma$ 's are usually thought of mathematically in the discrete-time (DT) domain, which means the majority of published designs are built using DT, e.g., switched-capacitor [3] or switched-current [4] circuitry. There is increasing interest in building  $\Delta\Sigma$ 's using continuous-time (CT) circuitry for the loop filter [5], [6], because it is generally possible to clock CT  $\Delta\Sigma$ 's at much higher frequencies than DT  $\Delta\Sigma$ 's. Then, for a given oversampling ratio (OSR), the conversion bandwidth can be greatly increased.

A typical circuit architecture for a high-speed CT  $\Delta\Sigma$  is depicted in Fig. 1. This is the double-integration modulator from [7], and it operates as follows. There are two integrator blocks with voltage inputs and outputs, each consisting of a transconductor for voltage-to-current conversion and a current integrator for current-to-voltage conversion. The quantizer is a latched comparator whose output drives differential pair DAC's; their output currents sum with the transconductor outputs. Thus, the feedback necessary for  $\Delta\Sigma$  operation works via Kirchhoff's current law (KCL).

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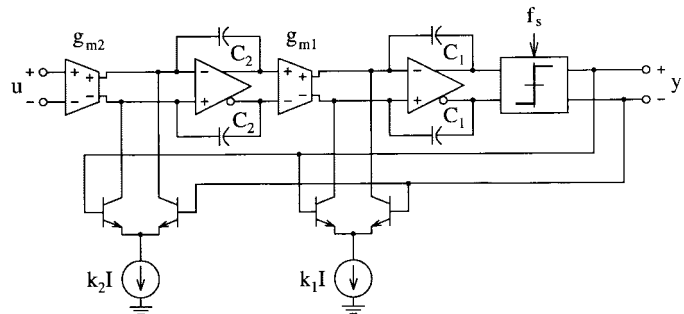


Fig. 1. Typical circuit architecture for a high-speed CT  $\Delta\Sigma$ .

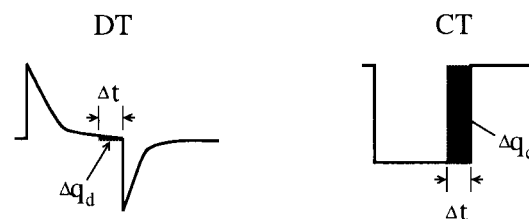


Fig. 2. Clock jitter effect in DT versus CT design.

Suppose there is timing jitter in the quantizer clock (clock jitter). On the left-hand side of Fig. 2, a typical feedback current waveform for a switched-capacitor (SC) DT  $\Delta\Sigma$  is depicted. Most of the charge transfer occurs at the start of the clock period, so that the amount of charge  $\Delta q_d$  lost due to a timing error is relatively small. By contrast, the right-hand side of Fig. 2 shows the DAC output current in a CT circuit such as Fig. 1; there, charge is transferred at a constant rate over a clock period, and so charge loss  $\Delta q_c$  from the same timing error is a larger proportion of the total charge. Moreover, in a DT design, jitter in the input sample-and-hold (S/H) clock means only the input waveform is affected. In a CT design, the sampling occurs at the quantizer rather than the input, which means the jitter affects the sum of the input plus quantization noise—a signal with considerably more power than the input alone. Hence, CT  $\Delta\Sigma$ 's are more sensitive to clock jitter than DT designs [8].

Clock jitter causes a slight random variation in the amount of charge fed back per clock cycle. Put another way, it is akin to adding a random phase modulation to the output bit stream. In an oversampled converter, the spectrum of the output stream is very noisy outside the (narrow) signal band; a random phase modulation causes the noise outside the signal band to fold into the signal band, raising the converter noise floor and degrading its resolution. The first aim of this paper is to quantify this

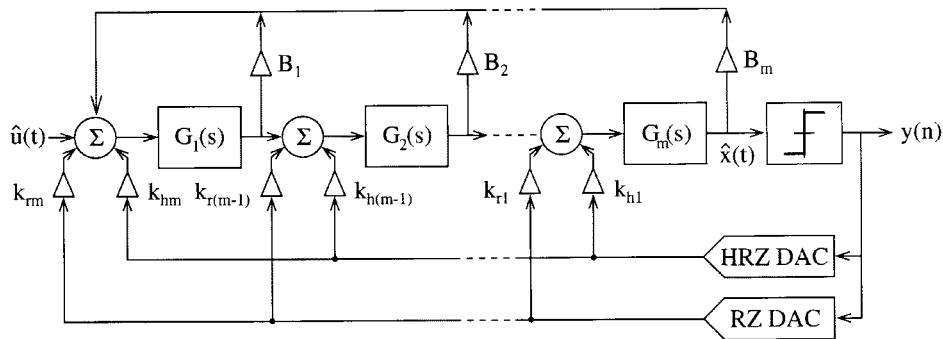


Fig. 3. Block diagram of general CT  $\Delta\Sigma$ M architecture.

degradation given a phase noise specification for a typical on-chip voltage controlled oscillator (VCO).

Even with a perfectly uniform sampling clock, it is nonetheless possible for there to exist a variation in the feedback charge. This happens because a real quantizer contains a regenerative circuit with a finite regeneration gain. Therefore, quantizer inputs with a magnitude near zero will take longer to resolve than inputs with a large magnitude—this is the classic problem of metastability in digital latches. In a  $\Delta\Sigma$ M, the input to the quantizer is decorrelated from the modulator input to the degree that it appears random; hence, the times when the quantizer input is near zero also appear random. This means that at certain unpredictable sampling instants, slightly more charge is transferred for the previous clock period, and slightly less for the next period. Again, the effect is to modulate out-of-band noise into the signal band and degrade converter resolution. The second aim of the present paper is to greatly expand on the authors' previous work in this area [9]: we wish to generalize our results to different orders of modulator and propose methods to overcome the effects of quantizer metastability.

This paper is organized as follows. Section II describes the modulator architectures considered here and the simulation program used to characterize modulator performance. Section III shows the effect of clock jitter on the output spectrum of a CT  $\Delta\Sigma$ M when the jitter instants are independent identically distributed (i.i.d.) random variables; Section IV treats the more practical case of jitter with a spectrum which resembles more closely that of real VCO phase noise. Section V discusses metastability in single-bit latched comparators, developing and validating the behavioral quantizer model used in the study of metastability in CT  $\Delta\Sigma$ M's. Section VI illustrates how performance is lost in CT  $\Delta\Sigma$ M's affected by metastability, and Section VII talks about methods for overcoming this loss. Section VIII estimates achievable modulator performance at a given quantizer clock speed in a given technology. Finally, Section IX draws conclusions about this work.

## II. PRELIMINARIES

A block diagram of the modulators which we study here is shown in Fig. 3. This is a generalization of Fig. 1 to  $m$ th order and is straightforwardly realizable in a fully integrated form using integrators for the gain blocks, or resonators if

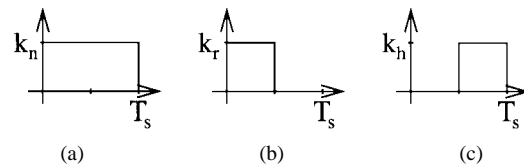


Fig. 4. Common practical DAC output waveforms. (a) NRZ. (b) RZ. (c) HRZ.

the modulator is bandpass (BP) rather than low pass (LP). The amplifiers can be built as transconductors, which means summation works by current summing. Most of the high-speed LP and BP modulators published so far (e.g., [5], [7], [10]–[12]) have been implemented more or less in this manner.

The gain blocks  $G_i(s)$  are generally integrators of the form  $A_i/sT_s$  in LP modulators and resonators  $A_i \cdot s/(s^2T_s^2 + \omega_i^2)$  in BP modulators. LP modulators often employ nonreturn-to-zero (NRZ) style feedback DAC's Fig. 4(a), though certain published "multifeedback" BP modulators for conversion at  $f_s/4$  require separate return-to-zero (RZ) and half-delayed RZ (HRZ) DAC pulses [Fig. 4(b) and (c)], hence their inclusion in the block diagram. The  $B_i$  feedbacks are for spreading the quantization noise zeros [13] which can result in significantly improved signal-to-noise ratios (SNR's) over coincident-zero modulators [2, Ch. 4].

Simulation is performed by integrating the time-domain state equations numerically using a variable time step fourth-order Runge–Kutta (RK4) method [14] in a C program. SNR is found from averaged periodograms of windowed output bit streams. The nonidealities of interest in this paper, sampling time jitter and quantizer metastability, are also implemented. The principal virtue of using C is that it executes quickly compared to, say, block diagram level simulations in Matlab or SPICE, though one might doubt that it can account for the dominant nonidealities that would be present in a transistor-level simulation. We allay these doubts in Section V.

## III. WHITE CLOCK JITTER

Suppose the sampling times for  $N$  output bits are given by

$$t_n = nT_s + \beta_n, \quad n = 0, 1, \dots, N-1 \quad (1)$$

and for the moment, let the  $\beta_n$  be i.i.d. random variables with variance  $\sigma_\beta^2$ . As noted in the Introduction, the effect of sample time jitter is to modulate the output spectrum out-of-band noise

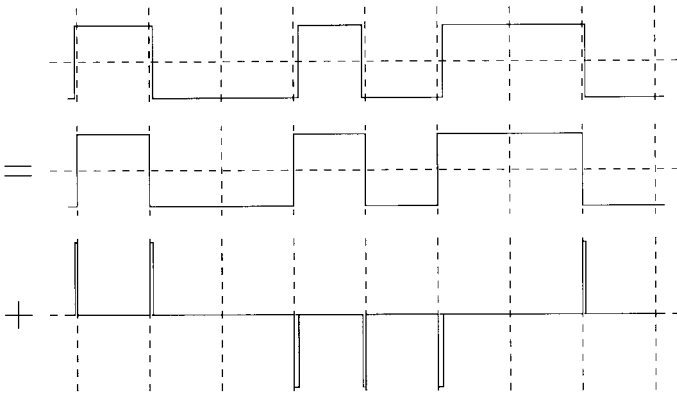


Fig. 5. Equivalent representations of a jittered bit stream.

into the signal band. This fills in the ideally infinitely-deep quantization noise notch with white noise, which lowers SNR and hence converter resolution. Let us quantify this statement for a couple of different cases.

#### A. LP Modulators with NRZ Feedback

This problem has been studied in the past [15], [16]; we review the results briefly here. The effect of jitter in an NRZ modulator can be explained by considering Fig. 5. The output bit stream with jitter shown in the top diagram is equivalent to the sum of an unjittered bit stream (the middle diagram) and a stream of pulses, which we call the *error sequence*, resulting from the jitter (the bottom diagram). By the linearity of the Fourier transform, the output spectrum for the top signal must equal the sum of the spectra of the bottom two signals. The error sequence can be represented by [15]

$$e_{\text{NRZ}}(n) = [y(n) - y(n-1)] \frac{\beta_n}{T_s} \quad (2)$$

where  $y(n)$  is the  $n$ th output bit. For wideband uncorrelated jitter, this error will be almost white, in which case we may write

$$\sigma_e^2 \approx \sigma_{\delta y}^2 \times \frac{\sigma_\beta^2}{T_s^2}. \quad (3)$$

In other words, the variance of the error sequence is the product of the variance of  $\delta y \equiv y(n) - y(n-1)$  and the jitter variance relative to the clock period. For  $N$  output bits, we expect the noise per periodogram bin to be

$$10 \log_{10} \left( \frac{2\sigma_{\delta y}^2 \cdot 2\sigma_\beta^2}{NT_s^2} \right) - 7.27 \text{ dB} \quad (4)$$

where the factors of two in the numerator arise because we are taking the one-sided power spectrum, and where 7.27 is the sum of  $10 \log_{10} 2 = 3.01$  dB (the power spectrum is root mean square (rms) power) and  $10 \log_{10} 0.375 = 4.26$  dB (0.375 is the gain of a Hann window). Moreover, if the SNR in baseband is completely limited by white jitter noise rather than noise-shaped quantization noise, then for an input

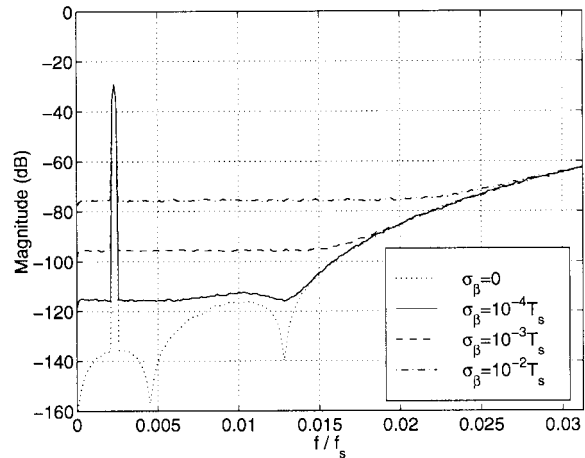


Fig. 6. Output spectrum for an NRZ LP modulator with white clock jitter.

amplitude  $V_{\text{in}}$ , we can write [15]

$$\text{SNR}_{\text{NRZ}} = 10 \log_{10} \frac{\text{OSR} \cdot V_{\text{in}}^2 / 2}{\sigma_{\delta y}^2 \left( \frac{\sigma_\beta}{T_s} \right)^2} \text{ dB}. \quad (5)$$

This is quickly verified in simulation. For a fifth-order modulator with NTF out-of-band gain 1.5, Chebyshev pole placement, and zeros spread optimally for  $\text{OSR} = 32$  [2, Ch. 4], the baseband spectra for various  $\sigma_\beta$  appear in Fig. 6. These simulations used  $N = 8192$  points and 256 averaged Hann-windowed periodograms were used to generate the spectrum. The input was  $-20$  dB, though it appears as  $-27.3$  dB in the spectrum because of windowing and because the spectrum is root mean square (rms). As an example, for  $\sigma_\beta = 10^{-2} T_s$ , (4) predicts a noise level per bin of  $-75.5$  dB (simulation found  $-75.8$  dB), and (5) predicts an SNR of 27.3 dB (simulation found 27.5 dB).<sup>1</sup>

#### B. Modulators with RZ and/or HRZ Feedback

Some LP modulators [17], [18], eschew NRZ DAC pulses for RZ pulses to reduce problems caused by unequal DAC edge rise and fall times, although a differential architecture such as that in Fig. 1 gets around these problems because differential signals are inherently symmetric [7]. We noted in Section II that BP modulators can be built using both RZ and HRZ DAC's in the same circuit. How does jitter affect the spectrum of a modulator using RZ (and possibly HRZ) DAC's?

Output spectra for simulations of two systems are shown in Fig. 7. Fig. 7(a) is for a double-integration LP modulator with RZ DAC's, and Fig. 7(b) is a fourth-order multifeedback BP modulator with a quantization noise notch at  $f_s/4$  using RZ and HRZ DAC's; its NTF was found by performing the substitution  $z^{-1} \rightarrow -z^{-2}$  in the NTF for a double-integration LP modulator [2, Ch. 9]. Once again, these are 256 averaged 8192-point Hann-windowed periodograms. For

<sup>1</sup>One reviewer observed that for large dc inputs, intuition suggests the noise due to jitter would decrease because there are fewer bit stream transitions and hence lower  $\sigma_{\delta y}$ . However, this does not increase modulator dynamic range because at zero input the maximum number of transitions occur.

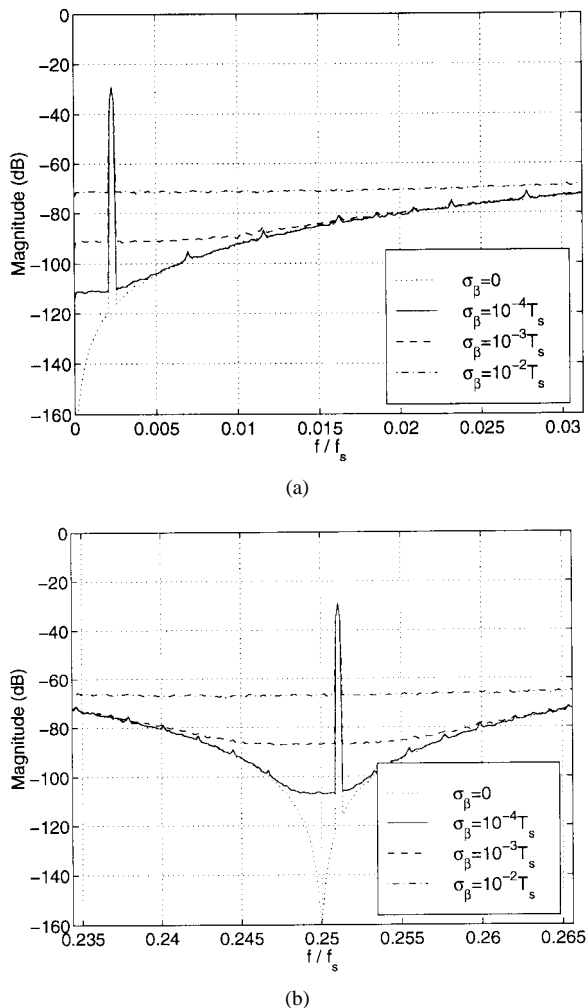


Fig. 7. Output spectra for (a) an LP RZ and (b) a BP RZ/HRZ modulator.

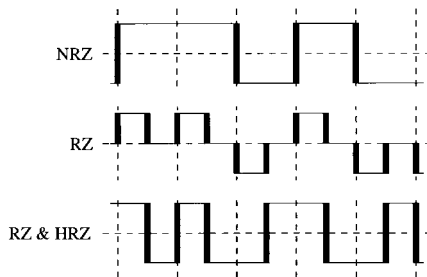


Fig. 8. Error sequence energy in different types of modulator.

a jitter standard deviation  $\sigma_\beta = 10^{-2}T_s$ , we find a baseband noise of  $-75.8$  dB per bin in a double-integration NRZ modulator, while for the LP and BP modulators in Fig. 7 the values are  $-71.3$  and  $-66.7$  dB, respectively.

The new values can be explained as follows. Fig. 8 shows the bit sequence  $\{+1, +1, -1, +1, -1\}$  as output by the same modulator with three different DAC's: NRZ, RZ, and a combination of both RZ and HRZ DAC's. The solid rectangles show edges which are affected by jitter. We may distinguish the three cases as follows.

- 1) In an NRZ modulator, jitter only matters when the output changes sign—the error sequence  $e_{\text{NRZ}}(n)$  is nonzero

only at those times, [cf. (2)]. The energy in the error sequence is proportional to  $\delta y^2 = [y(n) - y(n-1)]^2 = 4$  for a modulator with  $\pm 1$  outputs. For a double-integration NRZ modulator in we find  $\sigma_{\delta y} = 1.673$  in simulation, and the formula for variance is

$$\sigma_{\delta y}^2 = \frac{\sum \delta y^2 - \frac{(\sum \delta y)^2}{N}}{N-1} \approx \frac{4N_{\delta y}}{N} \quad (6)$$

for large  $N$ , where  $N_{\delta y}$  is the actual number of output bit transitions. Therefore  $\sigma_{\delta y}^2 = 2.80$  and we can estimate  $N_{\delta y}/N = \sigma_{\delta y}^2/4 = 0.70$  for such a modulator.

- 2) In an RZ modulator, both the rising and the falling edge of the pulse occur *every* clock cycle, so jitter affects a total of  $2N$  edges. The energy per edge is  $[\pm 1 - 0]^2 = 1$ , one quarter as much as in the NRZ case. But now, energy is being transferred over only half a clock cycle;  $\sigma_\beta$  is therefore twice as large relative to the energy transfer period in an RZ modulator.
- 3) In a modulator employing RZ and HRZ pulses of opposite sign, as is the case in a multifeedback BP modulator, there are now  $N$  edges at half clock cycles when going from the RZ to the HRZ pulse, and edges at half cycles where the output bits  $y(n-1)$  and  $y(n)$  are the same. These edges have energy 4 as in the NRZ case, and  $\sigma_\beta$  is twice as large relative to the energy transfer period as in the RZ case. In simulation, we find  $\sigma_{\delta y} = 1.405$  for the BP modulator, so that  $N_{\delta y}/N = 0.494$  from (6). The total number of edges is then  $N + N(1 - N_{\delta y}/N) = 1.506$ .

Taking all this into account, we may estimate an effective value of  $\sigma_{\delta y}^2$  in (3)

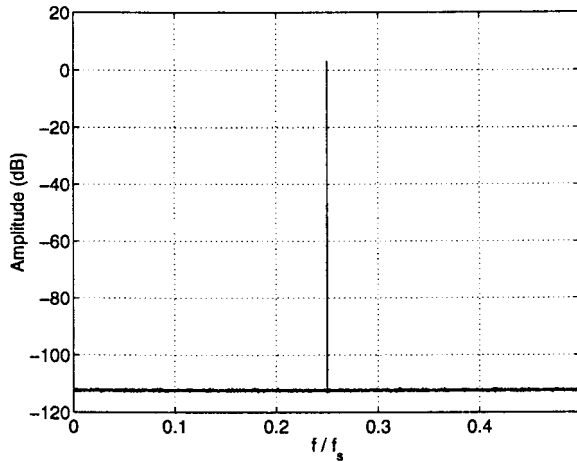
$$\sigma_{\delta y}^2 = \begin{cases} \frac{0.70N \times 4}{N} = 2.80, & \text{NRZ} \\ \frac{2N \times 1}{N} \times 2^2 = 8.00, & \text{RZ} \\ \frac{1.506N \times 4}{N} \times 2^2 = 24.10, & \text{RZ and HRZ.} \end{cases} \quad (7)$$

Therefore, we expect the RZ LP modulator to be  $10 \log_{10}(8.00/2.80) = 4.6$  dB worse than the NRZ LP modulator, and the BP modulator  $10 \log_{10}(24.10/2.80) = 9.3$  dB worse than the NRZ LP modulator. This is very close to what we observed (4.5 and 9.2 dB) in Fig. 7.

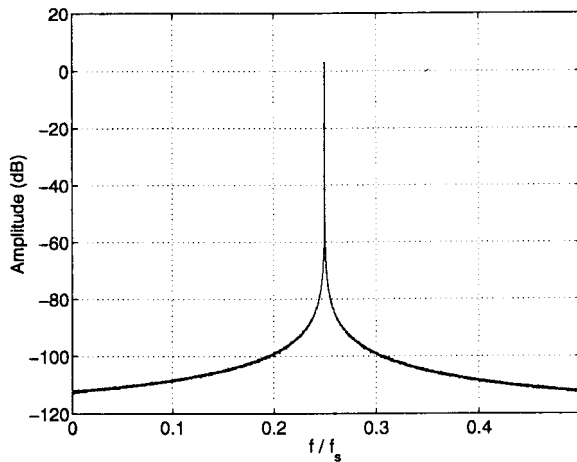
Generally, clock jitter affects RZ and/or HRZ modulators more severely than modulators employing just NRZ feedback. A good rule of thumb is: jitter noise will be 6 dB (1 bit) worse in the band of interest.

#### IV. VCO CLOCK JITTER

Although it is interesting didactically, the analysis in Section III is not terribly relevant in practice. The problem is, a real high-speed CT  $\Delta\Sigma\text{M}$  will likely be clocked on-chip with an integrated VCO, and sampling instants as given in (1) are not what a real VCO provides—the jitter instants  $\beta_n$  from a VCO are not well modeled as i.i.d. random variables. Fig. 9(a) shows 256 averaged 8192-point unwindowed periodograms



(a)



(b)

Fig. 9. Unwindowed spectra of sine wave carriers sampled with (a) independent and (b) accumulated jitter.

of a sine wave carrier sampled by an ideal S/H four times per period (i.e.,  $f_c = f_s/4$ ) with a jittered clock given by (1) and  $\sigma_\beta = 10^{-4}T_s$ . That kind of jitter, which we will denote *independent jitter*, adds white noise skirts to the carrier. A VCO produces skirts that are nonwhite.

#### A. Modeling VCO Phase Noise

We can modify (1) to produce nonwhite skirts fairly easily using a result due to Berkovitz and Rusnak [19]. Suppose the sampling instants are given by

$$t_n = nT_s + \sum_{i=0}^n \beta_i, \quad n = 0, 1, \dots, N-1 \quad (8)$$

where the  $\beta_i$  are still i.i.d. We denote this as *accumulated jitter* because it is a running sum, and a sine wave sampled four times per period with a jittered clock given by (8) has the spectrum shown in Fig. 9(b). Plotting the magnitude of the skirts relative to the carrier with a logarithmic frequency scale, as is customarily done in a VCO phase noise plot, yields the graph in Fig. 10, where we have assumed the sine wave has a frequency of  $f_c = 1$  GHz. The sideband power has a  $1/f^2$  dependence—exactly as it does in integrated VCO

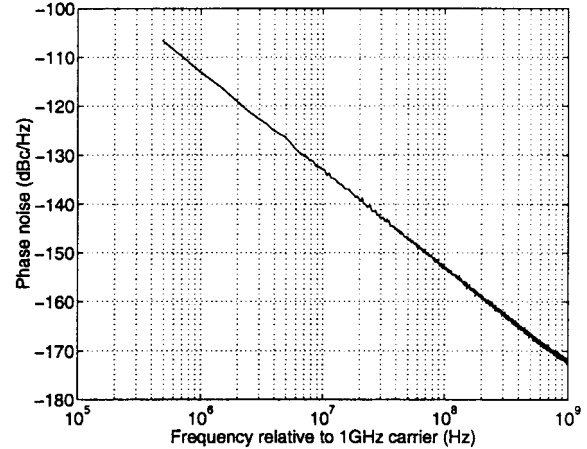


Fig. 10. Phase noise plot for accumulated jitter sampling of sine wave.

[20]. A VCO also has a  $1/f^3$  region close to the carrier, and a white noise floor far from the carrier, but (8) at least gives a reasonable approximation of a VCO phase noise over frequencies an intermediate distance from the carrier.

Phase noise in a VCO is usually specified as  $n_c$  dBc/Hz at an offset  $f_n$  from the carrier  $f_c$ . Happily, this  $f_n$  is usually in the  $1/f^2$  region of the phase noise. A typical achievable value of  $n_c$  is [21], [22]

$$n_c = -100 + 20 \log_{10} f_c \text{ dBc/Hz at 100-kHz offset} \quad (9)$$

for  $f_c$  in GHz. How can we relate this to  $\sigma_\beta$  in a  $\Delta\Sigma$ ? In Fig. 9(b), we had  $f_c/f_s = 0.25$ , and we find that altering the ratio  $f_c/f_s$  moves the phase noise in Fig. 10 proportionally to  $10 \log_{10} f_c/f_s$ . We wish for the sine wave being sampled (i.e., the “carrier”) to itself be the  $\Delta\Sigma$  clock, i.e., we desire  $f_c/f_s = 1$ . After some experimentation with normally-distributed  $\beta_n$ , it is found that using

$$\frac{\sigma_\beta^2}{T_s^2} \approx \frac{f_n^2 \times 10^{n_c/10}}{2f_c} \quad (10)$$

gives a phase noise of  $n_c$ , relative to the peak VCO height at  $f_n$  offset from  $f_c = f_s$ . We can therefore simulate the effect of clocking a  $\Delta\Sigma$  with a VCO meeting a certain phase noise spec by using sampling instants with accumulated jitter (8) and a variance given by (10).<sup>2</sup>

#### B. Effect of Accumulated Jitter on Performance

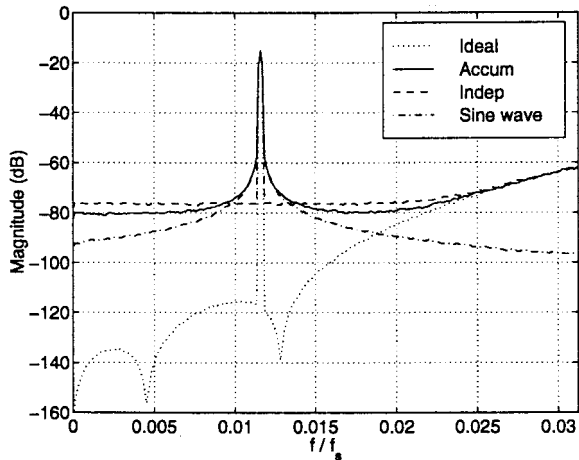
Example output spectra for two different types of modulator are depicted in Fig. 11. Fig. 11(a) is for the fifth-order Chebyshev NRZ modulator from Fig. 6, while Fig. 11(b) is for the fourth-order  $f_s/4$  multifeedback BP  $\Delta\Sigma$ 's from Fig. 7(b). Both simulations used  $\sigma_\beta = 10^{-2}T_s$ , and for contrast both independent *and* accumulated jitter spectra are plotted along with unjittered spectra.

There are two traits in the accumulated jitter spectra worth noting. First, accumulated jitter whitens the in-band spectrum in much the same way as independent jitter—this is not unexpected, because *any* clock spectral impurities will randomly modulate out-of-band noise into the signal band. The white

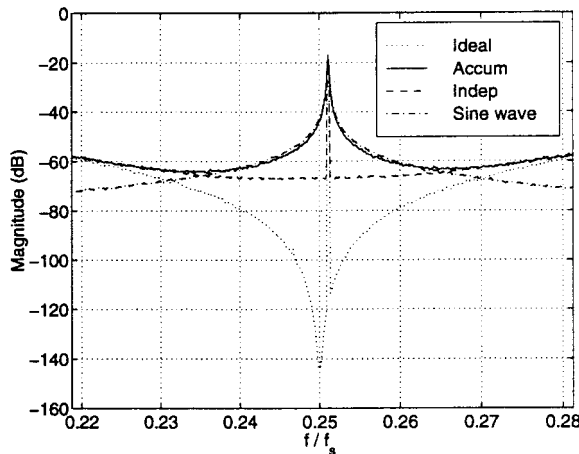
<sup>2</sup> $\sigma_\beta^2/T_s^2$  in (10) is dimensionless because  $10^{n_c/10}$  has units of  $\text{Hz}^{-1}$ .

TABLE I  
PERFORMANCE EFFECTS OF REAL VCO CLOCKING ON PRACTICAL MODULATORS

Modulator	$\sigma_\beta/T_s$	OSR	Ideal clock		VCO clock	
			DR	Peak SNR	DR	Peak SNR
1GHz 3rd order Butter	$2.236 \times 10^{-5}$	32	73.2dB	73.3dB	69.6dB	69.6dB
		64	93.5dB	93.8dB	90.5dB	89.2dB
2GHz 5th order Cheby	$3.155 \times 10^{-5}$	32	82.6dB	82.8dB	79.8dB	79.1dB
		64	114.5dB	100.7dB	101.6dB	92.1dB
3.2GHz double integ [7]	$3.953 \times 10^{-5}$	32	62.7dB	56.3dB	62.6dB	56.3dB
		64	78.8dB	71.3dB	79.0dB	71.4dB
4GHz 4th order BP [12]	$4.451 \times 10^{-5}$	32	63.2dB	56.4dB	63.2dB	52.7dB
		64	77.5dB	70.2dB	77.3dB	55.3dB



(a)



(b)

Fig. 11. Comparison of  $\Delta\Sigma\text{M}$  for independent and accumulated jitter, including spectrum of single tone at output of jittered S/H.

noise floor seems to be between about 1–5 dB lower for accumulated jitter compared to independent with the same  $\sigma_\beta$ ; for a given modulator, simulations shows this number is about constant for any values of  $\sigma_\beta$ , input frequency, and input amplitude. Second, the dashed–dotted lines on each graph show the spectrum of a sine wave with the same frequency as the input tone that has been sampled by a S/H circuit clocked with the same clock as the quantizer. The skirts on the tone appear directly in the output spectrum so long as they are higher than the white noise floor. This, too, is logical. Note the significance of the observation in Section IV-A that the skirt

height is proportional to  $10 \log_{10} f_c/f_s$ : as the input tone moves to higher frequencies, the skirts become higher relative to the tone. Thus, an LP modulator with a large tone close to the upper conversion band edge will have higher skirts and hence lower peak SNR than if the tone were close to dc. Moreover, the  $f_s/4$  BP modulator's performance is affected much more severely than the LP modulator, as is apparent in the graphs.

The  $\sigma_\beta$  used in Fig. 11 is unrealistically high for a practical VCO; it was used simply as an illustration. In Table I, we have shown how more realistic  $\sigma_\beta$  values would affect the performance of real high-speed CT  $\Delta\Sigma\text{M}$ 's. We have characterized the dynamic range (DR) and peak SNR of four modulators.

- 1-GHz-clocking third-order LP design with NRZ DAC pulses and Butterworth pole placement in the NTF with gain 1.5 and spread zeros;
- 2-GHz fifth-order LP design with NRZ DAC pulses and Chebyshev pole placement in the NTF with gain 1.5 and spread zeros;
- 3.2-GHz double-integration modulator published in [7], which has NRZ DAC pulses;
- 4-GHz fourth-order BP multifeedback modulator from [12] with a noise notch at  $f_s/4 = 1$  GHz. This modulator's intended application is for A/D conversion of 1-GHz RF signals, with subsequent mixing and signal processing performed in the digital domain.

For each modulator, we used (9) to pick a reasonable value of  $n_c$  given  $f_s$ , and (10) to find  $\sigma_\beta$ . Then, DR and peak SNR were measured from simulation of each modulator at two different OSR's, 32 and 64. The modulators were simulated both with ideal (unjittered) and VCO (jittered) clocks, and the input tone for the LP modulators is close to the upper band edge so that jitter skirts will be most pronounced.<sup>3</sup>

Looking at the table, we may make the following comments. The ideal modulators have DR and SNR limited by quantization noise only; for the modulators clocked with a VCO, the question is, does jitter noise impose additional performance

<sup>3</sup>A quick glance at the absolute  $\sigma_\beta$  values in the table makes them appear suspicious: for example, the 4-GHz modulator has  $T_s = 250$  ps and  $\sigma_\beta/T_s = 4.451 \times 10^{-5}$ , which means  $\sigma_\beta = 11.1$  fs. A typical gigabit-rate data generator specs edge jitter at a value of a few ps, two to three orders of magnitude higher than this  $\sigma_\beta$ . However, it must be remembered that we are using accumulated jitter, (8), not white. This means the clock phase over hundreds of cycles wanders significantly relative to a coherent reference; it is trivial to show that after  $N$  clock cycles, the phase is a Gaussian random variable with variance  $N\sigma_\beta^2$ . The  $\sigma_\beta/T_s$  values in the table are correct for a phase noise given by (9).

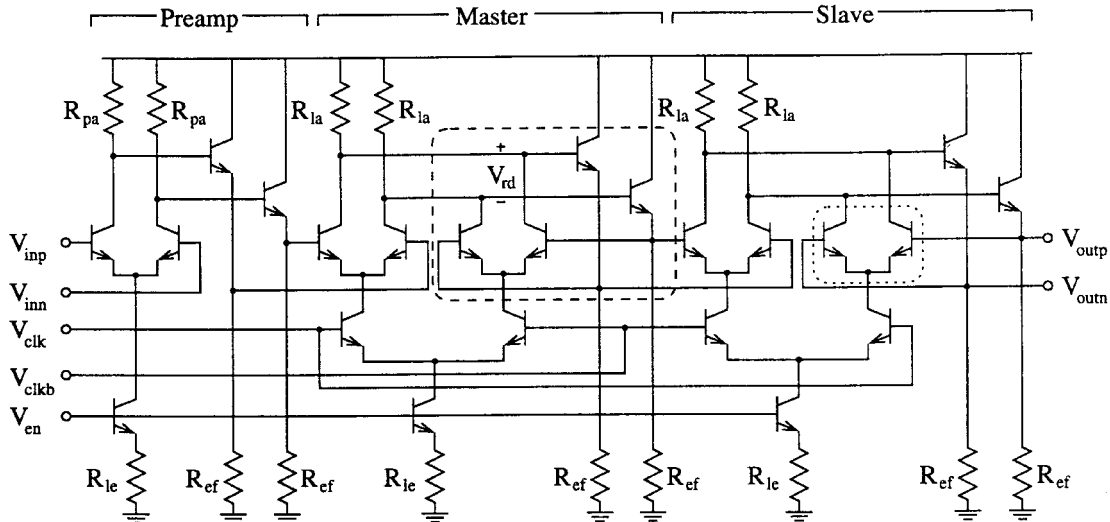


Fig. 12. Typical high-speed CT  $\Delta\Sigma$ M master-slave latched comparator with preamplifier. Dashed box highlights central regenerative circuit, dotted box transistors can be reconnected to make output return to zero.

limitations? For the double-integration modulator, the answer is no; performance is still quantization-noise limited for the realistic value of  $\sigma_\beta$  used. For high-order modulators and/or high OSR's, the likelihood of being jitter noise limited increases, as is particularly clear with the fifth-order modulator with OSR = 64: more than two full bits of DR are lost at this clock frequency. In addition, modulators with center frequencies away from dc suffer more greatly from jitter performance degradation, as we expect from Fig. 11—note that maximum SNR for the BP modulator is 4-dB worse than ideal at OSR = 32 and 15-dB worse at OSR = 64.

### C. Expected Performance Loss

An interesting thing happens when we combine the equations in this section to derive the maximum-achievable DR for a VCO-clocked modulator with a phase-noise spec given by (9). We assume that the in-band noise is completely white; the full calculation appears in Appendix A and the result is (23)

$$\text{Maximum DR (bits)} \approx 19 - 0.5 \log_2 f_N \quad (11)$$

where  $f_N$  is the Nyquist rate expressed in megahertz. This depends *only* on desired conversion bandwidth—it is independent of clock frequency so long as the VCO conforms to (9). As an example, a 32-MHz converter has  $f_N = 64$  MHz, and (11) says VCO jitter will limit the performance to no more than 16 bits in this band. But this is far more than the resolution achieved by published high-speed modulators. Clearly, VCO phase noise is unlikely to be the limiting factor in the performance of a high-speed modulator.

To conclude, the quality of integrated VCO's is good enough that the DR of only very high-resolution wideband LP  $\Delta\Sigma$ M's would likely be affected. Fast BP designs might be more problematic in terms of the peak SNR lost due to jitter skirts appearing on the output tone. For [12] which does band pass conversion at 1 GHz, we might think we can address this by downconverting to a frequency of a couple hundred MHz and doing the ADC there instead, where the jitter skirts in a  $\Delta\Sigma$ M

would be less severe; however, we must remember that the downconversion operation itself must be done with a jittered clock, and this introduces skirts on the tone in the mixing process.

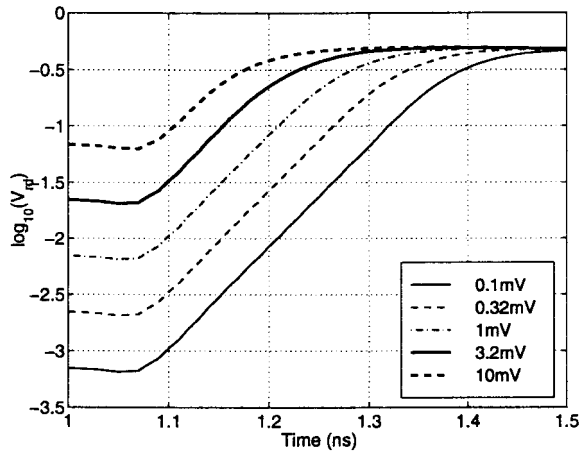
## V. LATCHES AND METASTABILITY

$\Delta\Sigma$ M's contain a quantizer, and the published high-speed CT  $\Delta\Sigma$ M's tend to be bipolar-only circuits with a one-bit quantizer. A typical quantizer for such circuits is shown in Fig. 12. It is an emitter-coupled logic (ECL)-style master-slave latched comparator with a preamplification stage. The dashed box contains the four transistors responsible for regeneration: when the circuit is enabled, the voltage difference  $V_{rd}$  at the bases of the emitter follower transistors is amplified by positive feedback until the maximum positive (digital +1) or negative (digital -1) voltage difference is reached.

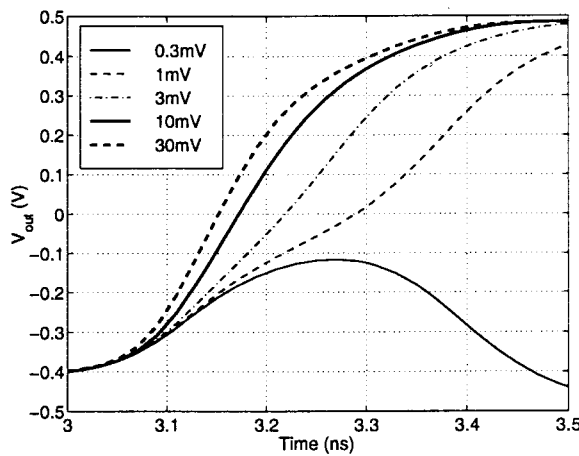
### A. Digital Circuits Versus $\Delta\Sigma$ M's

The usual analyses of metastability in digital latches [23], [24] treat the regenerative circuit as a single-pole system where the voltage difference at  $t = 0$  increases exponentially with a time constant inversely proportional to the gain-bandwidth (GB) product of the system. Such a treatment is valid here; Fig. 13(a) is a SPICE transistor-level simulation of just the master portion of Fig. 12 with input voltages given in the legend box. The differential pair amplifies the input voltage in the first half clock cycle, then the regenerative quad is enabled at  $T = 1$  ns and the value  $V_{rd}$  rises exponentially ( $\log V_{rd}$  is a straight line) until near the output voltage limit.

In digital circuits, the usual question to be answered is: what is the probability that the latch output is a valid digital level at time  $t$  given a certain setup time? In CT  $\Delta\Sigma$ M's, we are interested in a different question. Fig. 13(b) plots the output of a M/S latch whose input is first driven negative to make the latch output -1, then slightly positive to the value in the legend box. Note that the time when the latch output crosses zero on its way to +1 varies as a function of the positive input



(a)



(b)

Fig. 13. (a) Output of master stage only. (b) Output of M/S latch.

voltage (and that very small positive inputs cause the latch to produce a glitch). This output voltage drives the DAC's, and variations in its zero-crossing time (ZCT) have exactly the same effect as quantizer clock jitter—random edge variations modulate out-of-band noise into the signal band and whiten the spectrum. Thus, the question that concerns us is, what is the exact shape of the DAC output waveform? Most particularly, how do its ZCT and rise time vary for input voltages changing sign between clock periods?

### B. Characterization Method for $\Delta\Sigma M$ 's

In this paper, we determine the ZCT and rise time characteristics of a given latch from simulation. An analytic approach would be preferable, but finding one proved difficult; analyzing the latch output is one thing, but it is followed by a level-shifting follower and a DAC whose behavior must also be characterized. However, we show below that our empirical model works well. To apply it, a transistor-level SPICE file describing the complete feedback circuit (from latch input to feedback output) is composed. The input to the latch is made to be a piecewise-linear wave which first goes negative to drive the feedback output negative, then positive with slope  $v_{sl}$  so that at the next clocking instant the latch input is a specified

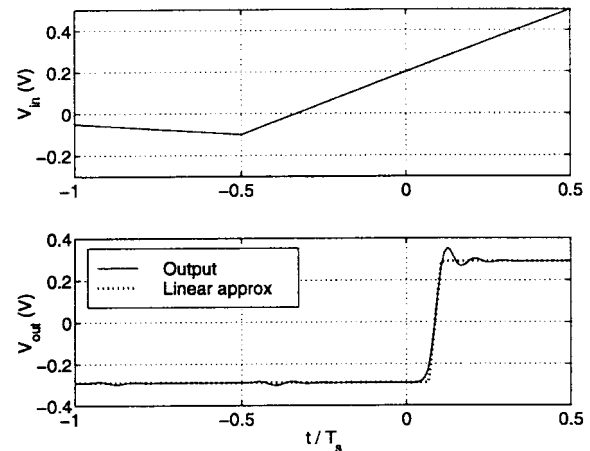


Fig. 14. SPICE input and output waveforms with linear approximation to output.

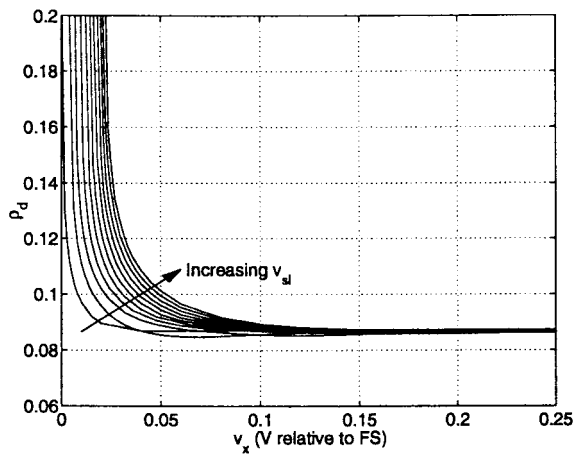
value  $v_x$ . For many different  $(v_x, v_{sl})$  pairs, the ZCT relative to the previous sampling instant (which we call  $\tau_d = \rho_d T_s$  for “delay time”) and the feedback output rise time (which we call  $\tau_r = \rho_r T_s$  for “rise time”) are found from simulation. If the circuit were single-ended rather than differential, it would be possible to characterize  $\rho_d$  and  $\rho_r$  both for rising and falling latch inputs.

An example of the process is illustrated in Fig. 14, which is for an M/S latch like Fig. 12, except without a preamplifier. The clock rate is  $f_s = 500$  MHz ( $T_s = 2$  ns), and the transistors have a switching speed of about  $f_T = 12$  GHz. In the upper graph, we see  $(v_x, v_{sl}) = (0.2, 0.6)$  for the input wave  $V_{in}$  at  $t = 0$ . The latch output goes through an emitter follower to a differential pair DAC whose collectors have been terminated with resistors. It is the differential resistor voltage that we plot as  $V_{out}$  in the bottom graph. We calculate  $(\rho_d, \rho_r) = (0.0860, 0.0386)$  and this is plotted as the dotted line in the bottom graph; the approximation to the actual waveform is quite good.

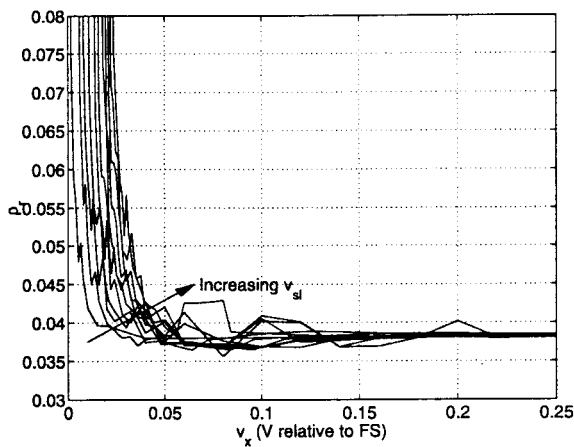
Using Perl [25] helps greatly to automate the procedure for many  $(v_x, v_{sl})$  pairs. Curves for  $\rho_d$  and  $\rho_r$  for our M/S latch and DAC's are plotted in Fig. 15. These curves indicate that for inputs close to zero, both the ZCT and the rise time increase, cf. Fig. 13(b). Moreover, for small enough inputs, no zero crossing is measured, which is what we saw with the glitch in Fig. 13(b) for  $V_{in} = 0.3$  mV—this is an example of quantizer hysteresis. And, as the input passes through  $v_x$  with higher slopes, delayed zero crossings and hysteresis happen for larger values of  $v_x$ . These curves have been normalized so that  $v_x$  is relative to the expected full-scale quantizer input, which for our example circuit, happens to be  $\pm 1$  V.  $v_{sl}$  values are normalized to full scale volts per clock period and swept from 0 to 2, which is more than enough to cover the range observed in an actual modulator.

The data from Fig. 15 is used as input to the RK4 simulation program; at each clocking instant, the program calculates  $(v_x, v_{sl})$  and uses linear interpolation to find  $(\rho_d, \rho_r)$ , which are then used to set the feedback pulse's delay time and rise time. Essentially, we are employing the technique of *behavioral modeling*.





(a)



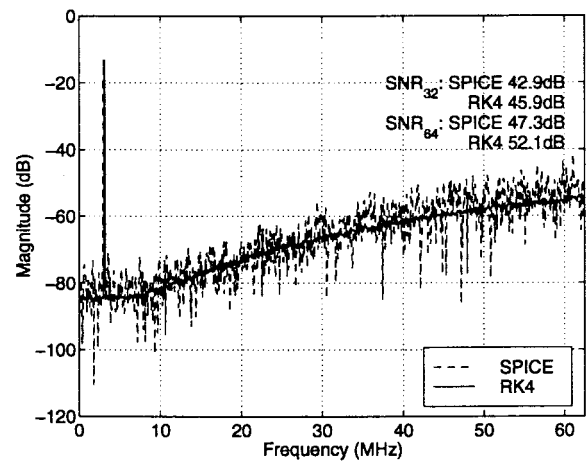
(b)

Fig. 15. Examples of  $\rho_d$  and  $\rho_r$  values, as characterized from simulation.

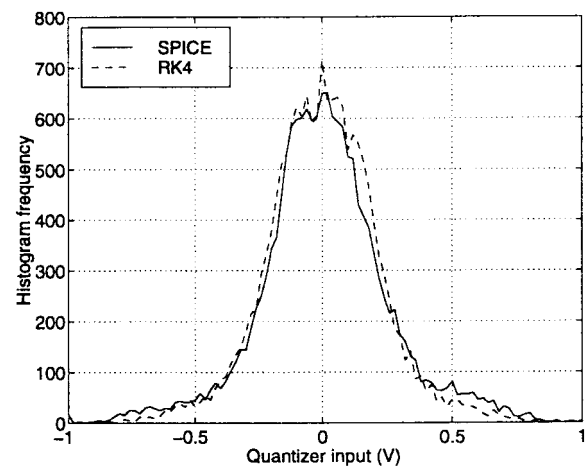
C. Validation of Quantizer Model

We wish to validate the use of our simulation program with the behavioral quantizer model as compared to full-circuit simulation in SPICE. The comparator and feedback circuitry of a double-integration modulator designed in a  $f_T = 25$ -GHz process clocking at  $f_s = 1$  GHz [26] were characterized as described in the previous subsection, and as many of the parameters from the actual circuit as possible (such as finite integrator gain and input resistance) were included in an input file to the RK4 simulator. For a  $-4$ -dB input at 3.1 MHz, the output spectra for a 16384-point SPICE simulation and 64 averaged 16384-point periodograms from the RK4 simulation are shown in Fig. 16(a). The spectrum details agree quite well, and there is acceptable agreement between calculated SNR values at OSR = 32 and 64, as shown on the graph. The RK4 program predicts a slightly lower white noise floor due to metastability than SPICE. Fig. 16(b) shows a histogram of the quantizer input pdf  $p_x(\alpha)$  from each simulator, and good agreement is seen—we are modeling the behavior and voltage levels in the real circuit quite well.

A dynamic range plot is shown in Fig. 17(a). The RK4 values of SNR were found from 32 averaged 4096-point periodograms, and in SPICE, each value was found from a single 4096-point simulation. The agreement between the two



(a)



(b)

Fig. 16. Comparison of SPICE and Runge-Katta simulation programs. (a) Output spectra. (b) Quantizer input pdf's.

is quite good, and while each RK4 simulation of 128k output bits took about 30 s, a single 4096-bit SPICE simulation took over four hours. Behavioral models are meant to increase simulation speed while maintaining accuracy, and we see that our quantizer model scores well on both counts.

D. Metastability Effect for Small Modulator Inputs

The dashed line in Fig. 17(a) has slope 1 dB/dB. This is the expected slope of the SNR versus input magnitude curve, and it is observed to hold true for large input amplitudes but not for small input amplitudes. We achieve SNR = 0 for an input magnitude of  $-42$  dB, whereas the dashed line predicts SNR = 0 at  $-52$ -dB input. With a  $-40$ -dB modulator input, the quantizer input as a function of time appears in Fig. 17(b); up to about sample 160, the quantizer behaves as it should, but then the modulator enters a  $\{+1, -1\}$  limit cycle from which it does not escape at a later time. Clearly, the modulator output no longer encodes the input signal at this point, which results in poor SNR. The authors observed this behavior in both RK4 and SPICE simulations.

It is known [27] that integrators with finite gain can cause such behavior. However, it was found in RK4 simulations with

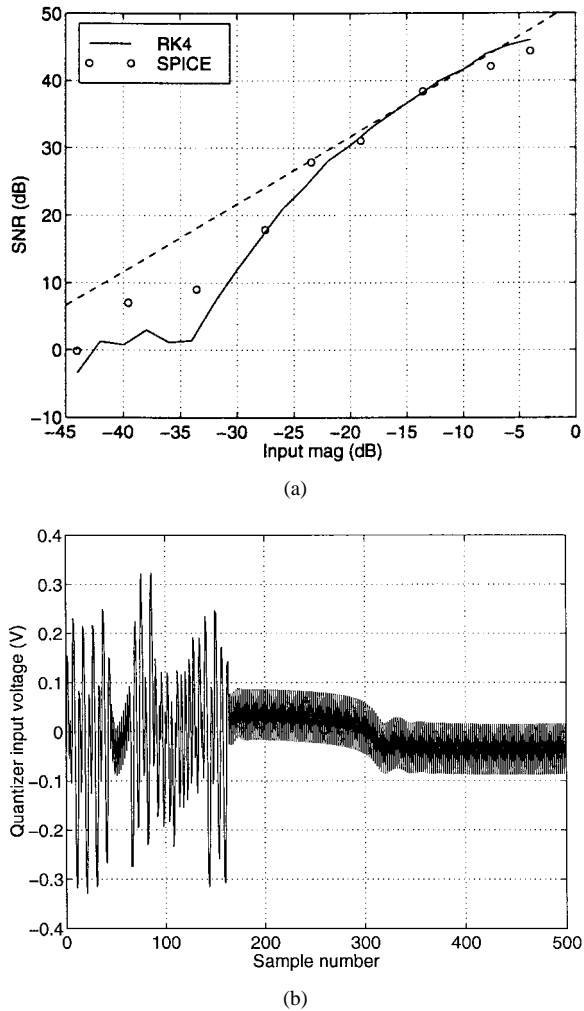


Fig. 17. Comparison of SPICE and Runge–Katta simulation programs. (a) Dynamic range plot. (b) Quantizer input limit cycle for low input magnitude.

a metastable quantizer that the behavior occurred even with infinite-gain integrators. The metastability is what is causing it in Fig. 17(b); from samples 160–300 or so, the bottom envelope of the quantizer input is near zero, which activates the metastability. It “escapes” from this mode of behavior only to have the *top* of the envelope approach zero and activate the metastability at sample 320. The metastability is excited alternately by the envelope top and bottom every few hundred cycles. We conclude that quantizer metastability can result in worsened sensitivity of an otherwise ideal CT  $\Delta\Sigma$ ’s to small input levels. This is, to the authors’ knowledge, a previously unpublished result.

## VI. REAL QUANTIZER PERFORMANCE EFFECTS

An ideal quantizer has the  $\rho_d$  versus  $v_x$  characteristic of Fig. 18(a). A practical quantizer exhibits various nonidealities as follows. Excess loop delay [Fig. 18(b)] is nonzero delay between the quantizer clock and the feedback output and is caused by finite transistor switching speed. It results in higher in-band quantization noise and worsened modulator stability, though its effects can be mitigated by feedback coefficient tuning [28]. Hysteresis [Fig. 18(c)] means the quantizer some-

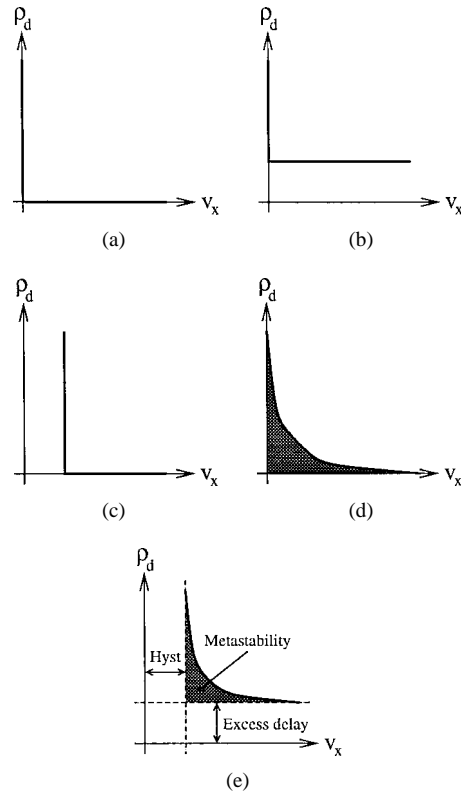


Fig. 18. Quantizer characteristics. (a) Ideal. (b) Excess delay. (c) Hysteresis. (d) Metastability. (e) Practical. Metastability severity is proportional to the area of the shaded region.

times does not make a decision to change the output bit when it should, but the performance of a  $\Delta\Sigma$  does not suffer much because of hysteresis [3]. Metastability [Fig. 18(d)] causes quantizer inputs near zero to take longer to resolve; metastability severity is proportional to the area under the curve. (A real quantizer, seen in Fig. 18(e), exhibits all three effects simultaneously, as we also saw in Fig. 15.) Quantizer metastability imposes two additional DR-limiting effects on top of those caused by excess loop delay and hysteresis. First, at low input amplitudes, there is the output limit cycle behavior mentioned in Section V-D. Second, at other input amplitudes, spectral whitening occurs—as we explained in the Introduction, metastability introduces a random variation in the feedback charge, and this folds out-of-band noise into the signal band in the same way clock jitter does.

The DR impact of using the quantizer characteristics in Fig. 15 on two different LP  $\Delta\Sigma$ ’s (a second-order and a fifth-order modulator) is shown in Fig. 19. In order to make the comparison fair, the modulators had their feedbacks scaled so that they all had the same quantizer input pdf standard deviation of  $\sigma_x = 1/3$ .<sup>4</sup> We observe the following.

- 1) An ideal modulator exhibits  $6m+3$  dB/oct improvement of SNR with OSR, where  $m$  is the modulator order [2, Ch. 4]. A modulator with a metastable quantizer will, for large enough OSR, be limited to a mere 3-dB/oct improvement because the noise notch in the output

<sup>4</sup>Since  $p_x(\alpha)$  is roughly Gaussian, fixing  $\sigma_x$  assures roughly the same distribution of abscissae in the quantizer characteristic in Fig. 15, and hence a roughly comparable ordinate distribution.

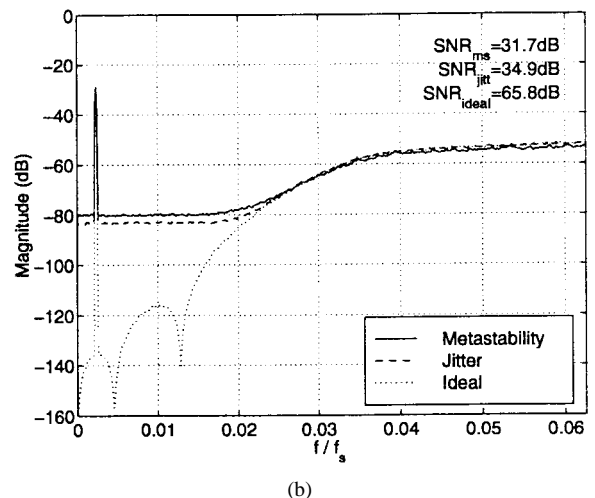
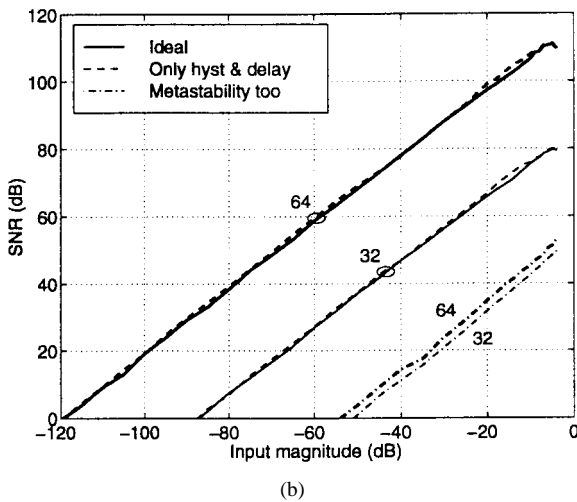
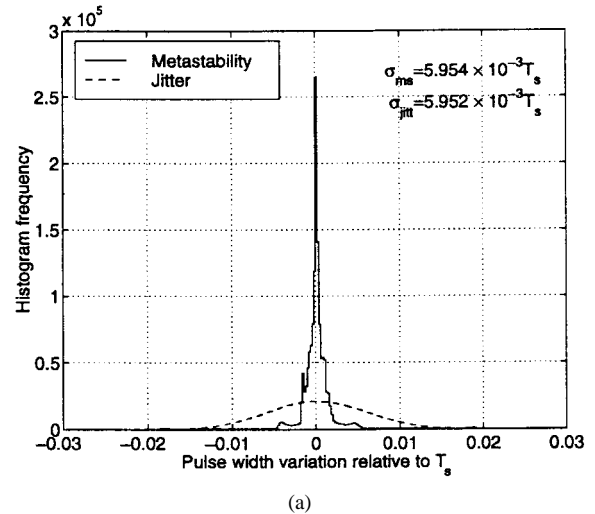
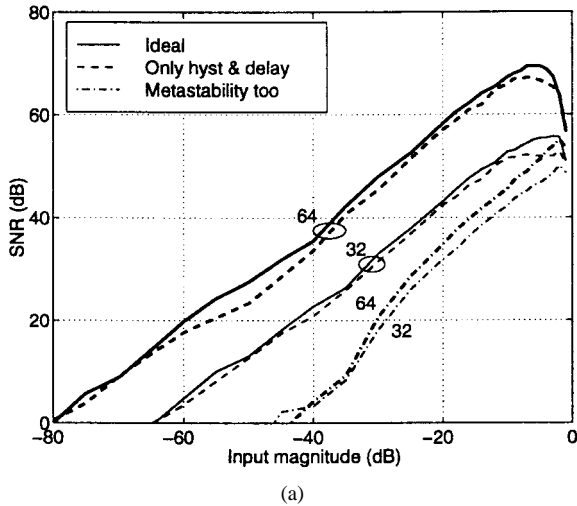


Fig. 19. Dynamic range plots. Numbers on curves are OSR values.

spectrum is filled in with white noise. For the quantizer in this example, going from OSR = 32 to OSR = 64 (shown by the dash-dotted lines) gives us only 3-dB SNR improvement. This means the DR at OSR = 64 is cut drastically, by a full factor of two.

- 2) The dashed lines show modulators with hysteresis and fixed  $(\rho_d, \rho_r) = (8.6\%, 3.9\%)$  (no metastability); compared with the ideal modulator, DR is hardly compromised at all, perhaps 0–3 dB depending on the modulator order.
- 3) The limit cycle behavior in  $\Delta\Sigma$ M's with metastable quantizers mentioned earlier affects lower order modulators more severely; the fifth-order modulator has 1-dB/dB slope all the way down to low input magnitudes, except perhaps for a dip near  $-35$  dB.

There is a relationship between performance lost by metastability and that lost by clock jitter, which can be explained as follows. We know that random variation in DAC pulse width (DPW) fills the output spectrum noise notch with white noise. The solid line in Fig. 20(a) shows a histogram of DPW variation for the fifth-order modulator with an ideal sampling clock and a metastable quantizer with characteristic given by Fig. 15. The standard deviation of this distribution

Fig. 20. Comparison of clock jitter to quantizer metastability. (a) DAC pulse width variation histogram. (b) Output spectrum.

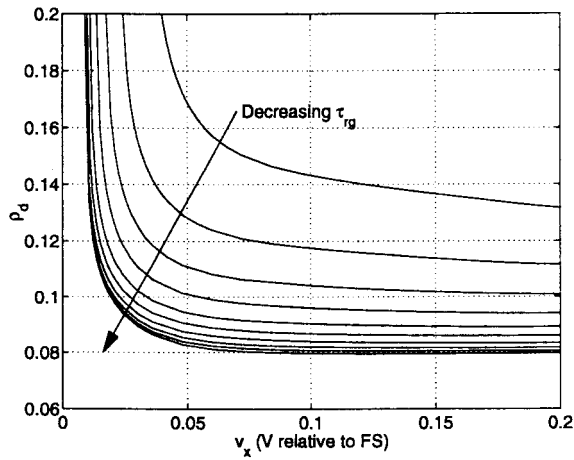
is  $\sigma_{ms} = 5.95 \times 10^{-3} T_s$ . To get the same DPW variance from a modulator with an ideal quantizer and a clock with independent jitter, we must set the jitter variance to

$$\sigma_{\beta} = \sigma_{ms} / \sqrt{2}. \quad (12)$$

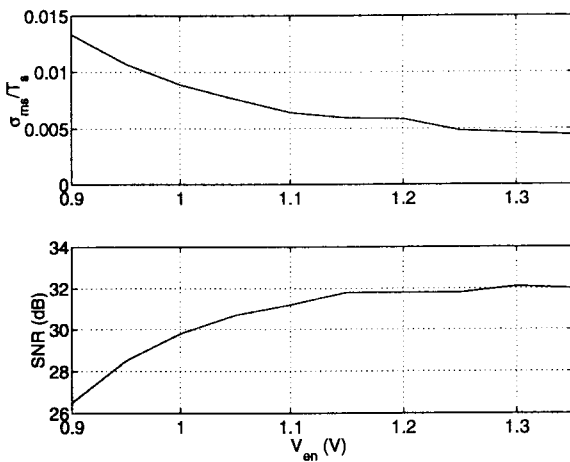
This results in the dashed-line histogram in Fig. 20(a). Note that  $\sigma_{jitt} \approx \sigma_{ms}$ . Since the DPW variance is about the same in both cases, Section III-A taught us that the spectrum whitening should also be about the same. Fig. 20(b) illustrates this to be the case; the SNR value for the modulator with the metastable quantizer is 31.7 dB, while that for the modulator with clock jitter is 34.9 dB. The noise floors are close, but not identical, because the distribution of the DPW histogram for a metastable quantizer is not particularly Gaussian. Still, the agreement is quite good.

## VII. MITIGATING METASTABILITY PERFORMANCE LOSS

To overcome the performance penalties imposed by quantizer metastability, we must consider the source of the loss: the variations in the DPW caused by finite regeneration speed. We observed in Section VI that this variance  $\sigma_{DPW}$  is related to the area under the metastability curve in Fig. 18(e), or



(a)



(b)

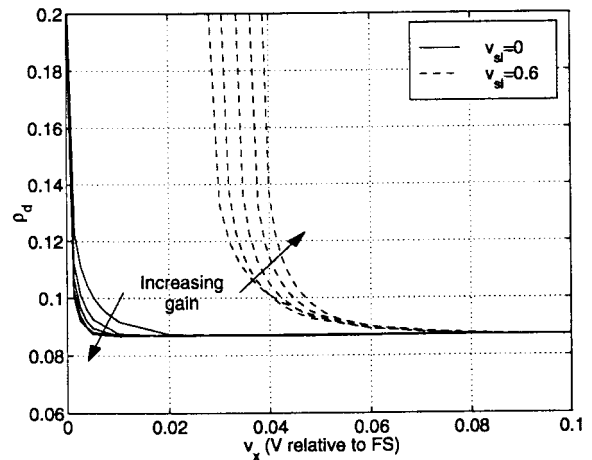
Fig. 21. (a) Quantizer metastability curves. (b) Modulator performance as a function of  $\tau_{rg}$ .

equivalently the “sharpness” of the corner in the curve. There are several approaches we might take to reduce its area or increase its sharpness.

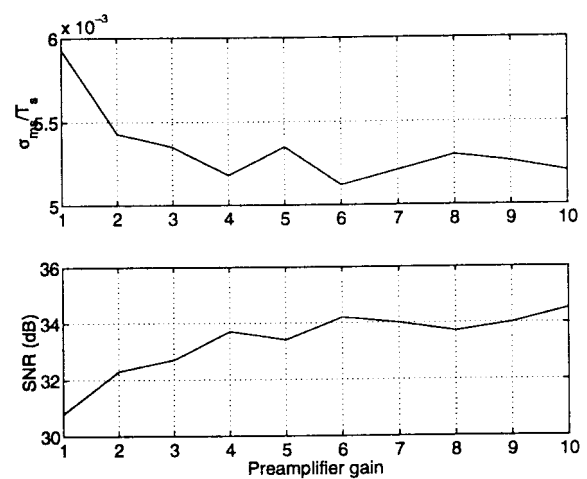
#### A. Regeneration Time

In Section V-A we said that the regeneration time of a latch is inversely proportional to the GB product of the regeneration circuit. If we were to increase this GB product, the corners of the metastability curves would become sharper as follows: the slope of the curves in Fig. 13(a) would increase, which in turn would, we hope, mean that it would take a *smaller* input level  $v_x$  for the curves in Fig. 13(b) to exhibit increased delay—in other words, for the set of  $v_x$  values in that legend box, the rising output edges would be bunched more closely together. In turn, the curves in Fig. 15 would rise toward infinity more abruptly, i.e., the corner becomes more pronounced.

One way to affect the regeneration time constant  $\tau_{rg}$  of the latch in Fig. 12 is to change the current in the regenerative quad; this is accomplished by altering the voltage  $V_{en}$ . To keep the comparison reasonable, we will adjust  $V_{en}$  and  $R_{da}$  simultaneously to keep the latch output voltage swing at around  $\pm 300$  mV. Fig. 21(a) shows quantizer metastability curves for  $v_{sl} = 0.6$  as  $V_{en}$  changes over the range 0.90–1.35



(a)



(b)

Fig. 22. (a) Quantizer metastability curves. (b) Modulator performance as a function of preamplifier gain.

V. There is some sharpening of the corner with increased  $V_{en}$ , but as an added bonus, also lower  $\rho_d$  and hysteresis. Just as diminishing returns are apparent there, so too are they in Fig. 21(b), where the SNR is plotted against  $V_{en}$ . The optimum SNR does not quite occur where  $\tau_{rg}$  is a minimum, which happens to be at  $V_{en} = 1.15$  V—very minor improvements are obtained as  $V_{en}$  is raised further because latch output slew rate continues to increase with  $V_{en}$ .

#### B. Preamplification

Our latch has consisted of simply the master and slave stages so far, but we might think to add one or more amplification stages prior to the master stage. Traditional analyses show that for cascaded amplifiers, there exists an optimum gain per stage that maximizes the overall amplifier GB product, and hence, the amplifier speed. Depending on the assumptions made, the optimum gain is either  $e = 2.72$  [29, Ch. 2] or  $\sqrt{e} = 1.65$  [30, Ch. 8]. In the present circuit, we will consider only one preamplifier stage and study how its gain affects metastability performance.

Fig. 22(a) shows metastability curves for a quantizer with a simple differential pair preamplifier as depicted in Fig. 12. The

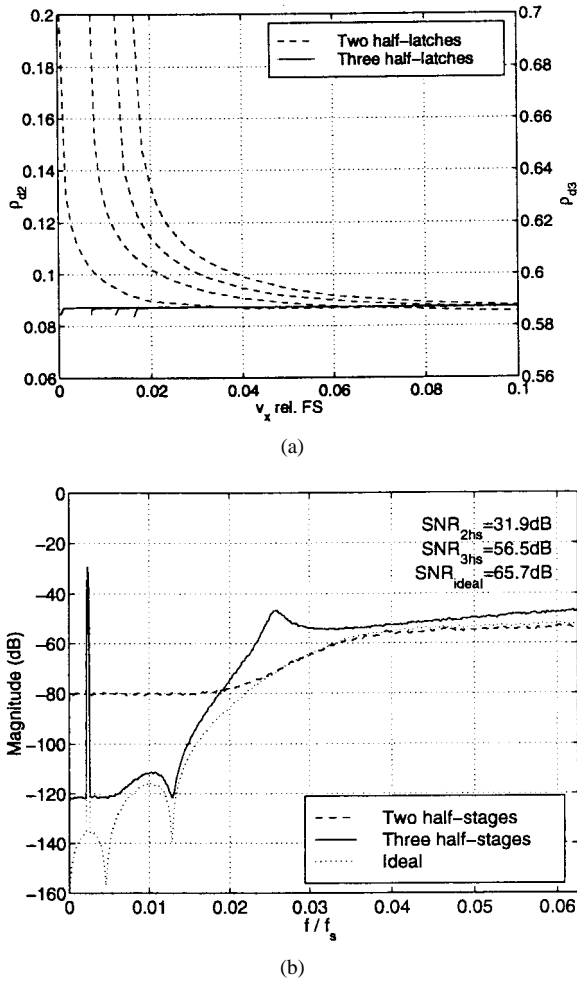


Fig. 23. (a) Quantizer metastability curves. (b) Output spectrum for quantizer with an additional latching stage.

gain was varied between 1 and 10 by changing the value of  $R_{pa}$ . Increasing the gain has the desirable effect of sharpening the corner of the metastability curves for constant quantizer inputs (see the solid lines in the figure), but for *slewing* inputs, little sharpening can be seen as gain rises. Hysteresis increases slightly with gain, and in fact, it has increased substantially over Fig. 21(a) from about 10 to about 30 mV. This is not terribly detrimental to performance, as we said in Section VI. Fig. 22(b) shows that a preamplifier offers about 2 dB of SNR improvement. There is little point in using a gain above four, it appears.

### C. Additional Latching Stages

A third thing we can try is using additional latching stages after the slave stage in Fig. 12 [7]. Clocking each stage on the opposite clock phase from the previous stage gives the previous stage a good deal of time to settle. The drawback is that each latching stage adds half a sample of delay in the feedback loop, and this delay is detrimental to modulator stability and dynamic range [28]. However, we can somewhat overcome these problems by tuning the  $k$  feedback parameters.

Fig. 23(a) shows quantizer metastability curves for the baseline latch with only master and slave half-stages, and a second latch that has a third half-stage following the slave

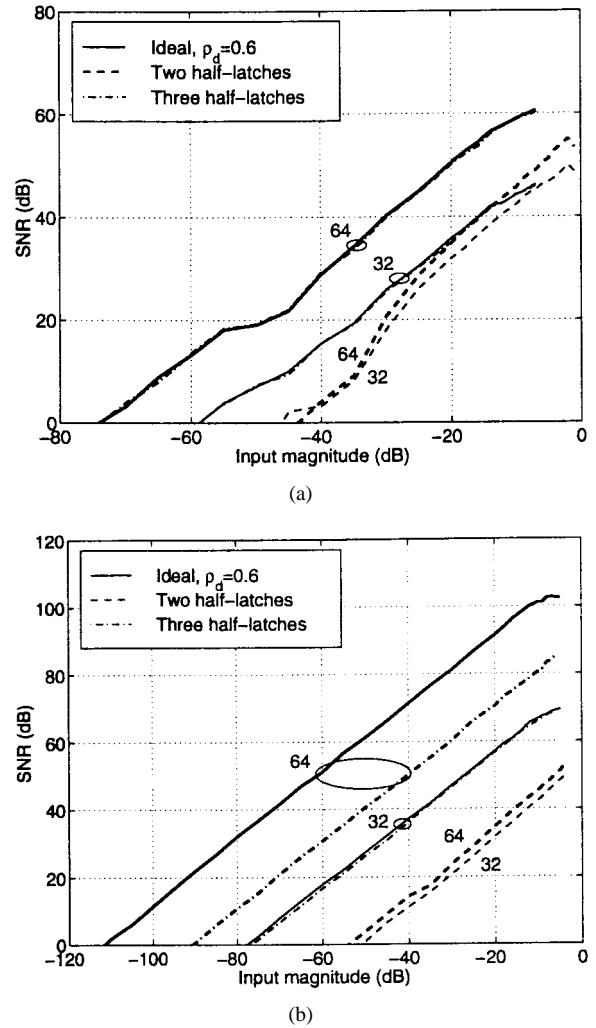


Fig. 24. Dynamic range plots. Numbers on curves are OSR values.

which is clocked on the same phase as the master. We have added one half sample of extra delay, as can be seen on the right  $y$  axis where  $\rho_{d3}$  is 0.5 more than  $\rho_{d2}$  on the left axis, but the variation of  $\rho_{d3}$  with  $v_x$  is drastically reduced. This results in a huge improvement—about 40 dB—in the white noise floor of the output spectrum, Fig. 23(b). From simulation, we find DPW variance has dropped nearly two orders of magnitude, from  $5.9 \times 10^{-3}T_s$  to  $1.4 \times 10^{-4}T_s$ . The fifth-order modulator was unstable with  $\rho_d = 0.6$  and nominal  $k$  values, but the  $k$ 's were tuned so that the modulator was stable and the DR of a modulator with an ideal quantizer was maximized at  $\rho_d = 0.6$ . One artifact of the large  $\rho_d$  is the peak in the spectrum at  $0.025f_s$ , something which is caused by the movement of the equivalent NTF loop filter poles toward the unit circle as excess loop delay increases.

Fig. 24 shows DR plots for the two LP  $\Delta\Sigma$ 's from Fig. 19 contrasting performance with an ideal quantizer and the two quantizers with the metastability curves in Fig. 23(a). With two half-latches, there is only about 10% excess delay, but the third-half latch pushes that up to 60%. A modulator with an ideal quantizer and 60% delay usually requires feedback  $k$  tuning to remain stable, and even then, the DR is less than for the 10% delay case. However, when the ideal quantizer is

TABLE II  
PERFORMANCE OF LP MODULATORS WITH TWO- AND THREE-HALF LATCHES AGAINST IDEAL

Modulator	OSR	Ideal $q$ , $\rho_d = 0.0$		Two half-latch		Ideal $q$ , $\rho_d = 0.6$		Three half-latch	
		DR	Peak SNR	DR	Peak SNR	DR	Peak SNR	DR	Peak SNR
Double integration	32	64dB	56dB	45dB	50dB	52dB	46dB	52dB	46dB
	64	79dB	69dB	43dB	55dB	67dB	61dB	67dB	60dB
3rd order Butter	32	74dB	68dB	49dB	52dB	66dB	61dB	66dB	61dB
	64	95dB	89dB	51dB	55dB	88dB	83dB	84dB	81dB
4th order Butter	32	78dB	74dB	48dB	51dB	68dB	65dB	67dB	65dB
	64	105dB	99dB	50dB	54dB	95dB	91dB	85dB	85dB
5th order Cheby	32	83dB	80dB	47dB	50dB	73dB	69dB	72dB	69dB
	64	116dB	111dB	50dB	53dB	107dB	103dB	85dB	85dB

replaced with a metastable one, the three half-latch quantizer is the clear DR winner. Table II summarizes the results for four cases: an ideal quantizer, a quantizer with two half latches, an ideal quantizer with 60% excess loop delay and tuned  $k$ 's to maximize DR, and a quantizer with three half latches and the same tuned  $k$ 's. For high-order modulators with high OSR, the white noise resulting from metastability is what limits the achievable performance, though much less severely when with three rather than two half latches.

#### D. Other Modulator Architectures

In Section III-B, we noted that RZ LP and multifeedback BP modulators suffer one bit worse performance in the presence of clock jitter. However, both styles of modulator can be useful for reducing metastability performance loss.

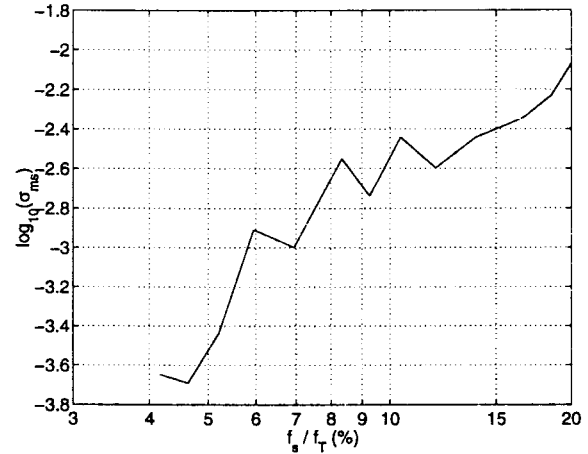
In the case of RZ LP modulators, we can insert a half-sample delay in the feedback, but still have the DAC return to zero after one half clock cycle; this would result in an HRZ LP modulator with DAC pulses like that in Fig. 4(c). It is trivial to choose feedback coefficients for such a modulator that builds a noise transfer function identical to that for a double-integration  $\Delta\Sigma M$  [6].

For the specific case of an  $f_s/4$  BP modulator, the loop filter has a two-sample delay in the numerator (i.e., the coefficient of  $z^{-1}$  is zero). This means we are permitted to insert a full sample of delay in the feedback path while still getting stable fourth-order noise shaping [31]. This is accomplished with two additional half-latch stages; this is even more helpful than a single half-latch for reducing metastability, and so should be used in any  $f_s/4$  BP CT  $\Delta\Sigma M$ .

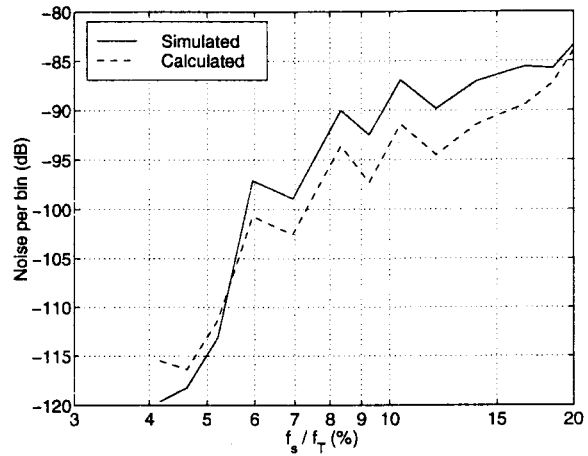
#### VIII. MAXIMUM NRZ LP CLOCKING FREQUENCY

In our LP NRZ examples so far, we have been clocking at  $f_s = 500$  MHz in a  $f_T = 12$  GHz technology. At faster sampling rates, two things together limit resolution. First, the transistor switching time starts to become a larger fraction of a clock period. This means the excess loop delay  $\rho_d$  and DAC pulse rise time  $\rho_r$  start to increase. There comes a point when excess loop delay makes the modulator completely unstable and impervious to stabilization through feedback coefficient tuning. Second, the metastability behavior of even the three half-latch comparator will start to degrade.

Fig. 25(a) shows  $\sigma_{ms}$  as a function of  $f_s$  with both variables on a log scale. This was found from simulating the fifth-order LP NRZ modulator with feedbacks tuned for optimal DR at



(a)



(b)

Fig. 25. Effect of increasing  $f_s$  on (a)  $\sigma_{ms}$  and (b) calculated and simulated noise level.

the given clock frequency over the range 500 MHz to 2.5 GHz, and finding the variance of the DPW histogram like the one in Fig. 20(a). Using those same simulations with an OSR of 32 at clock frequencies from 500 MHz to 2.5 GHz yields the in-band white noise level per bin shown in Fig. 25(b). This agrees to within 3 dB with the calculated value from (4) where  $N = 8192$ ,  $\sigma_\beta$  is found from (12), and  $\sigma_{\delta y} \approx 1.1$  is found from simulation. The modulator goes unstable at  $f_s = 2.5$  GHz due to excess delay and no amount of feedback tuning seems to restore stability.

We can use the data in Fig. 25 to come up with an approximate rule of thumb for the maximum performance

achievable with a three-half latch quantizer assuming in-band noise is dominated by white noise due to metastability and three transistors (output follower, level-shifting follower, and DAC differential pair) in the feedback path. The calculation is shown in Appendix B, and the results are (29) and (31)

$$\begin{aligned} \text{DR} &\geq 11.5 + 0.5 \log_2 \text{OSR bits}, & f_s/f_T &\leq 5\% \\ \text{DR} &\approx 8.5 + 0.5 \log_2 \text{OSR} + \log_2 \frac{f_s/f_T}{5} \text{ bits}, & f_s/f_T &\geq 6\%. \end{aligned} \quad (13)$$

This tells us that clocking slower than about 5% of  $f_T$  is recommended if we desire at least 14-bit performance with a reasonable OSR like 32 or 64; better performance can be achieved with a slower clock or more oversampling. Clocking faster than 5% or so of  $f_T$  means we are limited to 12-bit or worse performance at the same OSR's. We do not recommend clocking faster than  $f_s = 0.2f_T$  under any circumstances, since stability will be questionable at best and nonexistent at worst at such high speeds.

In closing this section, we must comment further on (13). First, it gives an upper bound on DR; DR will be limited either by white noise due to metastability *or* quantization noise, depending on the OSR chosen. Second, it is not continuous; it has a jump between 5% and 6%. Third, the bound is not tight, for  $f_s/f_T < 5\%$  improves as we slow the clock down, though because of the semi-empirical nature of the calculations, we cannot easily extrapolate below this point. We estimate that metastability will have a negligible effect in most modulators when  $f_s/f_T < 2\%$ .

## IX. CONCLUSION

Jitter which causes a variation in the width of the DAC pulses in a CT  $\Delta\Sigma$  degrades modulator performance by whitening the in-band noise. Quantizer clock jitter and quantizer metastability are the two major mechanisms which cause this. We have derived one simple equation for each mechanism which allows estimation of maximum achievable performance. If building an integrated  $\Delta\Sigma$  with an on-chip clock generated from a VCO, a properly designed VCO should not cause a problematic level of jitter, though very high-resolution modulators or those with a center frequency away from dc might suffer. For quantizers, a three half-latch design is recommended for reducing adverse metastability effects over a simple master/slave design. Clocking faster than about 5% of  $f_T$  will limit performance to at most 12 bits in modulators with moderate OSR's. Higher resolutions can be obtained by oversampling more or clocking more slowly.

### APPENDIX A DERIVATION OF $\Delta\Sigma$ VCO PHASE NOISE LIMITED PERFORMANCE

We derive the maximum-achievable DR for a CT  $\Delta\Sigma$  clocked by a VCO with a phase noise given by (9). First, we start with (4), which is the in-band white noise level for a

modulator with independent jitter and  $N$  bins

$$10 \log_{10} \left( \frac{2\sigma_{\delta y}^2 \cdot 2\sigma_{\beta}^2}{NT_s^2} \right). \quad (14)$$

We have omitted the  $-7.27$  dB, because that is needed only for the rms Hann-windowed periodogram. If the in-band noise were white over the entire band, whose width expressed in bins is

$$N/(2 \cdot \text{OSR}) \quad (15)$$

then the total in-band noise would be the argument of  $\log_{10}$  in (14) times (15)

$$10 \log_{10} \left( \frac{\sigma_{\delta y}^2 \cdot 2\sigma_{\beta}^2}{\text{OSR} \cdot T_s^2} \right). \quad (16)$$

The quantity  $\sigma_{\delta y}$  in (16) is found in simulation to have a value between 1 and 2, so assume

$$\sigma_{\delta y} \approx 1.5 \quad (17)$$

on average. From (10), and also from the second column of Table I, we can find that

$$\frac{2\sigma_{\beta}^2}{T_s^2} = 10^{-12} f_s, \quad f_s \text{ in MHz.} \quad (18)$$

Substituting (17) and (18) in (16), and recalling from Fig. 11 that accumulated jitter tends to give white noise levels 1–5 dB (say 3 dB on average) lower than independent jitter, yields

$$10 \log_{10} \left( \frac{1.5^2}{\text{OSR}} \times f_s \times 10^{-12} \right) - 3 \approx -120 + 10 \log_{10} \frac{f_s}{\text{OSR}} \quad (19)$$

as the total in-band noise. The DR is then the maximum allowable signal amplitude (MSA) minus (19), where MSA for typical modulators lies between  $-1$  and  $-5$  dB or so [15]. Assume

$$\text{MSA} \approx -3 \text{ dB} \quad (20)$$

on average, and note that

$$f_N \equiv \frac{f_s}{\text{OSR}}, \quad (21)$$

Using (20) and (21) with (19) gives

$$\begin{aligned} \text{DR} &\approx -3 - (-120 + 10 \log_{10} f_N) \\ &= 117 - 10 \log_{10} f_N \text{ dB}, \quad f_N \text{ in MHz} \end{aligned} \quad (22)$$

$$\approx 19 - 0.5 \log_2 f_N \text{ bits}, \quad f_N \text{ in MHz} \quad (23)$$

where in writing (23) we have used the fact that each bit of resolution corresponds to 6.02 dB of DR.

APPENDIX B  
DERIVATION OF  $\Delta\Sigma$ M METASTABILITY  
LIMITED PERFORMANCE

Here we find the maximum-achievable DR for a CT  $\Delta\Sigma$ M with a three half-latch single-bit quantizer as a function of  $f_s/f_T$ . Looking at Fig. 25(b), there appear to be two distinct regions in the curve, one for  $f_s/f_T < 5\%$  or so and one for  $f_s/f_T > 5\%$ . In the first case, the in-band noise per bin is  $-115$  dB or less in an 8192-point simulation; a single bin thus corresponds to  $OSR = 4096$ . If the noise were completely white, then each doubling of the OSR would raise the total noise by 3 dB. Extrapolating this in the opposite direction allows us to find the total in-band noise of

$$-79 - 3 \log_2 OSR \quad (24)$$

when  $f_s/f_T < 5\%$ . For the opposite case, the noise starts at  $-97$  dB/bin when  $f_s/f_T = 6\%$  and increases roughly at 6 dB/oct with  $f_s/f_T$ . Assuming white in-band noise leads to a total noise of

$$-61 - 3 \log_2 OSR + 6 \log_2 \frac{f_s/f_T}{5}. \quad (25)$$

DR is given by MSA minus total noise. We can see in Fig. 24 that a modulator with half a sample of feedback delay typically has an MSA between  $-10$  and  $-6$  dB; assume

$$MSA \approx -8 \text{ dB} \quad (26)$$

on average.

Combining (26) with (24) tells us that

$$DR \geq -8 - (-79 - 3 \log_2 OSR) \quad (27)$$

$$= 71 + 3 \log_2 OSR \text{ dB}, f_s/f_T \leq 5\% \quad (28)$$

$$= 11.5 + 0.5 \log_2 OSR \text{ bits}. \quad (29)$$

The  $\geq$  sign in (27) is because the noise in (24) is worst-case, for  $f_s/f_T = 5\%$ ; at slower clock speeds, the in-band noise will be lower and DR higher. Using (26) and (25) gives

$$\begin{aligned} DR &\approx -8 - \left( -61 - 3 \log_2 OSR + 6 \log_2 \frac{f_s/f_T}{5} \right) \\ &= 53 + 3 \log_2 OSR - 6 \log_2 \frac{f_s/f_T}{5} \text{ dB}, f_s/f_T \geq 6\% \end{aligned} \quad (30)$$

$$= 8.5 + 0.5 \log_2 OSR + \log_2 \frac{f_s/f_T}{5} \text{ bits}. \quad (31)$$

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**James A. Cherry** (S'97–M'98), for a photograph and biography, see p. 389 of the April 1999 issue of this TRANSACTIONS.

**W. Martin Snelgrove** (M'81), for a photograph and biography, see p. 389 of the April 1999 issue of this TRANSACTIONS.