A Linear Integrated *LC* Bandpass Filter with *Q*-Enhancement

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Abstract—A technique is proposed in this paper for linearizing active Q-enhanced monolithic LC filters. This technique employs capacitive dividers and tunable linear transconductors. Various multi-tanh translinear circuits can be used to implement the linear transconductors, taking into consideration the need for linear operating range and the low supply voltage. A linear Q-enhanced LC filter using the proposed technique has been implemented in a 0.5- μ m bipolar process. The demonstrated filter chip operates at a center frequency around 1 GHz with the quality factor tunable up to 400 without spurious oscillation. For a Q of 40, the input intercept point and spurious-free dynamic range are -6.67 dBm and 36 dB, respectively, at a power consumption of 68 mW and with 7 dB of gain.

Index Terms—Analog filters, continuous-time circuits, monolithic inductors, RF IC's, wireless IC's.

I. INTRODUCTION

The rapid growth in wireless telecommunication systems has necessitated research and development of monolithic bandpass filters for gigahertz radio frequencies. Active analog filters using popular techniques such as active-RC, MOSFET-C, and switched-capacitor are still far from reaching such a high frequency. Transconductor-C filters are fast but have poor dynamic range when designed for gigahertz frequencies. There has been great interest in building LCbandpass filters using monolithic inductors on silicon [1]-[3]. LC filters can be used as image reject filters at the front end of a wireless transceiver [4] or as inside sigma-delta modulator loops for gigahertz bandpass analog-to-digital conversion [5]. It has been shown that Qenhanced LC filters provide an improvement of Q_o^2 in dynamic range over comparable transconductor-C filters, where Q_o is the quality factor of the inductor without enhancement [6]. Monolithic silicon inductors are lossy and generally exhibit a quality factor less than 10 at gigahertz frequencies. Losses in monolithic inductors can be compensated by the addition of active circuitry in positive feedback to increase the quality factor of the overall LC bandpass filter at the cost of nonlinear distortion due to the exponential I-V characteristic of the amplifier, typically an emitter-coupled differential pair. Linearity is vital in filter design for wireless receivers since signals from strong interferers may otherwise combine by intermodulation to mask a desired signal.

In this paper, we present an approach to improve the linearity of active Q-enhanced LC filters by using capacitive dividers and linear bipolar differential transconductors. Modified multi-tanh doublets [7] using series-connected diodes are proposed to implement the transconductors to achieve a wide linear range. Experimental results for a linear Q-enhanced LC filter fabricated using a 0.5- μ m silicon bipolar process are reported.

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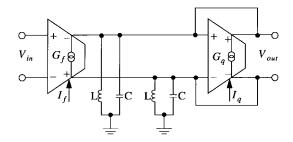


Fig. 1. Configuration of active Q-enhanced LC filters.

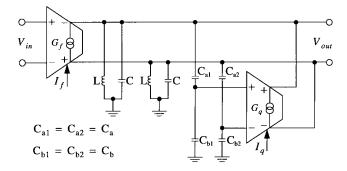


Fig. 2. Linearized active Q-enhanced LC filter configuration.

II. THE LINEARIZATION TECHNIQUE

The idea of active Q-enhancement for LC filters is to place the lossy monolithic inductors in a positive feedback loop to realize high Q filters as shown in Fig. 1. Transconductor G_f injects the input signal to the resonators. Transconductor G_q is placed in positive feedback to operate as a negative resistor for compensating the loss of the inductor. Both transconductors need to be linearized to make the filter exhibit good linearity, especially transconductor G_q since a high Q filter may result in a large output signal. Further, G_q has to be variable to tune Q over process and temperature variation. Implementation of the transconductor using a Gilbert gain cell plus emitter degeneration can greatly improve linearity but with a significant noise penalty, a poor tuning range and a much larger power consumption. The dynamic range is worse than that of a simple differential pair even though the linear range can be enlarged. Transconductors implemented using multi-tanh translinear circuits have excellent tunability and are not noisy; but the achievable linear operation range is still limited, typically less than 100 mV_{pp} [7].

In addition to multi-tanh linearization, we use capacitive voltage dividers formed by (C_{a1}, C_{b1}) and (C_{a2}, C_{b2}) shown in Fig. 2 to scale the filter output voltage down to an acceptable level for linear operation of the positive feedback transconductor G_q . This lets us maintain large signals on the core resonator to control noise without overdriving the amplifier. To derive the transfer function of the filter, an equivalent block diagram is drawn in Fig. 3. Z(s) represents the LC tank as illustrated in the figure, taking into account the loss of the inductor that is modeled by R_p . It can be shown that

Z(s) =

$$\frac{R_p L(C_1 + C_b)s}{R_p L[C(C_a + C_b) + C_a C_b]s^2 + L(C_a + C_b)s + R_p(C_a + C_b)}$$
(1)

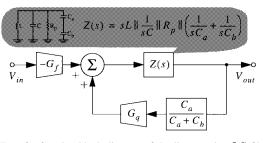


Fig. 3. Transfer function block diagram of the linear active-LC filter.

From the block diagram, we have

$$V_{\text{out}}(s) = \left[-G_f V_{\text{in}}(s) + G_q \frac{C_a}{C_a + C_b} V_{\text{out}}(s) \right] \cdot Z(s)$$
 (2)

Rewriting the equation

$$\frac{V_{\rm out}(s)}{V_{\rm in}(s)} = -\frac{(C_a + C_b)G_f Z(s)}{(C_a + C_b) - C_a G_q Z(s)}$$
(3)

Substituting Z(s) from (1), we obtain the second-order filter transfer function

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{\frac{C_a + C_b}{C(C_a + C_b) + C_a C_b}G_f s}{s^2 + \frac{C_a + C_b - C_a R_p G_q}{R_p [C(C_a + C_b) + C_a C_b]}s + \frac{C_a + C_b}{L[C(C_a + C_b) + C_a C_b]}} \tag{4}$$

Comparing the above equation with the standard bandpass filter transfer function

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -A_0 \left(\frac{\omega_0}{Q}\right) s \left/ \left[s^2 + \left(\frac{\omega_0}{Q}\right) s + \omega_0^2 \right] \right.$$
(5)

we obtain midband gain A_0 , center frequency ω_0 and quality factor Q, respectively,

$$A_{0} = \frac{(C_{a} + C_{b})R_{p}G_{f}}{C_{a} + C_{b} - C_{a}R_{p}G_{q}}$$
(6)

$$\omega_0 = \sqrt{\frac{C_a + C_b}{L[C(C_a + C_b) + C_a C_b]}} \tag{7}$$

$$Q = \frac{R_p [C(C_a + C_b) + C_a C_b]}{C_a + C_b - C_a R_p G_q} \omega_0.$$
 (8)

III. LINEAR TRANSCONDUCTOR DESIGN

The objective of the transconductor design is to achieve linear operation for as large an input signal amplitude as possible, while keeping the added noise and the power consumption as small as possible. The transconductors and the capacitive dividers need to be designed properly. Compared to emitter degeneration, the multi-tanh technique extends the linear operation range with (theoretically) 3 dB less added noise and allows variable transconductance through control of the tail current. This combination of linearity and tunability is what is needed for the positive feedback transconductor G_q . The feedfoward transconductor G_f can be designed using either emitter degeneration or a multi-tanh circuit because tunability is not essential.

A conventional multi-tanh transconductor cell is composed of two or more unbalanced emitter-coupled differential pairs in parallel and in cross-connections of input terminals and output terminals [7]. An offset is created for each unbalanced differential pair. The offset value is determined by the emitter-area ratio between the

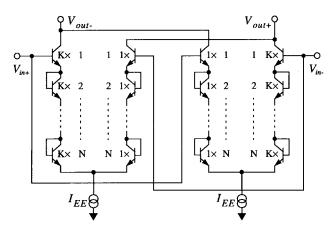


Fig. 4. Series-diode-connected doublet configuration.

two transistors. The transconductance for each differential pair is symmetrical with respect to the input voltage around the offset voltage, and monotonically decreases as the input voltage becomes larger or smaller than the offset. The combination of these differential pairs with weighting of their tail currents can produce a relatively flat transconductance over the range from the most negative offset voltage to the most positive offset voltage, which defines the linear input range of the transconductor. To make the linear range and the transconductance of the design less dependent on the manufacturing process, one additional consideration in this work is to have the emitter-areas of the transistors used in the transconductors be integer multiples of a unit transistor. Unit transistors can thus be used to make the integer-ratioed transistor by connecting them in parallel [8] and ratios can be expected to be relatively independent of process. Similarly, it is also our object that all tail currents have the same value or are the integer magnitudes of the unit tail current. Based on these considerations, the achievable linear operation range of the conventional multi-tanh technique is very constrained. The linear operation range is about 40 $\,{\rm mV_{pp}}$ for a multi-tanh doublet (two differential pairs), and 50 $\,{\rm mV_{pp}}$ for a multi-tanh triplet (three differential pairs) at 1% transconductance fall-off based on SPICE simulation and analytical analysis. One limitation of multi-tanh circuits is that these circuits have residual nonlinearities with a "multiple bumps" shape, and going to extreme ratios increases swing at the cost of making the "bumps" larger and worsening linearity within the "linearized" range. The tradeoff is similar to that between ripple and cutoff in a Chebyshev filter design.

To further improve the usable signal swing, the emitter-coupled differential pair can be degenerated by adding 2(N-1) diodes in series between the emitters of input transistors. Using diodes rather than resistive degeneration allows us to maintain tunability. Fig. 4 shows a series-diode-connected doublet. It consists of two unbalanced series-diode-connected emitter-coupled pairs connected in parallel. The offset voltage created by proportioning the respective emitter areas between the unit transistor and the ratioed transistor with a ratio of K for a simple unbalanced differential pair is $V_{\rm off} = V_T \ln K$, where $V_T = kT/q \approx 26$ mV is the thermal voltage for room temperature. The differential output current, $I_{\rm out}$, for the tansconductor can be derived as

$$I_{\rm out} = I_{EE} \left\{ \tanh\left(\frac{V_{\rm in} - NV_{\rm off}}{2NV_T}\right) + \tanh\left(\frac{V_{\rm in} + NV_{\rm off}}{2NV_T}\right) \right\}$$
(9)

Taking the derivative of the above equation, we obtain the transconductance, which can be written as

$$G = G_1 + G_2 \tag{10}$$

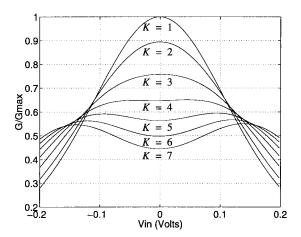


Fig. 5. Transconductance characteristics with different emitter-area ratios.

where

$$G_1 \approx \frac{I_{EE}}{2NV_T} \operatorname{sech}^2\left(\frac{V_{\mathrm{in}} - NV_T \ln K}{2NV_T}\right)$$
 (11)

and

$$G_2 \approx \frac{I_{EE}}{2NV_T} \operatorname{sech}^2\left(\frac{V_{\mathrm{in}} + NV_T \ln K}{2NV_T}\right)$$
 (12)

representing the transconductance of the left differential pair and the transconductance of the right differential pair, respectively. From the above equations, it can be seen that the peak of G_1 shifts $NV_T \ln K$ to the right of the origin, and the peak of G_2 moves $NV_T \ln K$ to the left of the origin. The combination of G_1 and G_2 results in a linear range between the two peaks. Increasing the value of N would result in a larger separation of the peaks of G_1 and G_2 , and therefore a larger linear range would be generated at the cost of linearity between the peaks. Figs. 5 and 6 give the SPICEsimulated transconductance characteristics while varying K and N, respectively. From observation of the shape of the curves in Fig. 5, it is clear that K = 4 results in the flattest curve between the two peaks. From Fig. 6, we can see that the linear range is increased as expected by increasing the number of diodes in series with the trade-off of a reduction of transconductance value in the linear range. This confirms an analytical expression for the transconductance in the linear range obtained from the Taylor expansion of G at $V_{in} = 0$, which is

$$G^{0} = \frac{4KI_{EE}}{NV_{T}(1+K)^{2}}$$
(13)

N is, however, limited by the power supply voltage. For a 5-V power supply, the maximum number of diodes that can be used in cascode is about 4, i.e., N = 5.

Ignoring the noise correlation between the tail currents, the noise analysis of the series-diode connected multi-tanh doublet is straightforward. Summing the two identical noise generators from the left-hand and right-hand differential sections in power, we have the input referred noise voltage

$$\frac{\tilde{V}_n}{\sqrt{\Delta f}} \approx \sqrt{kT \frac{N(1+K)^2}{K} \left(2R_{bb} + \frac{V_T}{E_{EE}}\right)}$$
(14)

where R_{bb} is the base resistance of the transistors. Combining (13) and (14) gives

$$\frac{\tilde{V}_n}{\sqrt{\Delta f}} \approx \sqrt{\frac{4kT}{G^0}} \left(1 + \frac{2R_{bb}}{V_T/I_{EE}}\right) \tag{15}$$

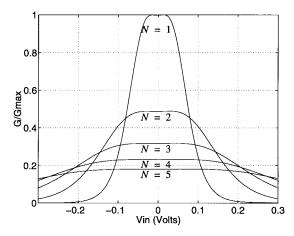


Fig. 6. Transconductance characteristics with K = 4 and different values of N.

which tells us that the noise is determined by the G^0 required to compensate losses and that transistors with low R_{bb} allow us to approach the limit.

IV. LINEAR ACTIVE-*LC* FILTER PROTOTYPE AND EXPERIMENTAL RESULTS

Linear active-LC filter design using conventional multi-tanh translinear circuits for implementing G_q requires a large capacitor ratio for the capacitive dividers and more than three differential pairs with much large emitter-area-ratioed transistors to achieve a wide linear operation range. The advantage is that the resulting filter can operate at a very low supply voltage, which can be as low as 1 V. Low power consumption can then be expected. The design using the series-diode-connected doublet trades supply voltage for linearity, which results in larger power consumption. Another way of looking at this is that designing a low-voltage circuit for the same dynamic range as our part would require use of lower impedance levels to reduce resonator kT/C and kTL noise, which in turn would call for higher currents at no net gain in power consumption.

To investigate the utility of the proposed linearization approach, a linear active-LC bandpass filter was designed. Fig. 7 shows the circuit schematic. The circuit gives a second-order bandpass filter response with its Q tunable through the feedback transconductance G_q and is designed to operate at a 5-V power supply. The seriesdiode-connected multi-tanh doublet was chosen for both feedfoward and feedback transconductors with K = 4 and N = 3. To reduce the noise contribution of the parasitic base resistance, large transistors are preferred in the transconductor design. We selected the monolithic inductors from a library, choosing one with an intrinsic Q as high as possible to achieve a large dynamic range. The capacitors were designed using a metal-insulator-metal structure to achieve the best quality factor and the best tolerance. Two identical capacitors are connected back-to-back in parallel as shown in the figure to maintain balance in the presence of substrate parasitics. To reduce the substrate coupling effects, an n+ subcollector region under the capacitors was used to shield them from the substrate. The dc bias voltages V_{D1} and V_{D2} of the capacitive voltage dividers are set by the voltage bias circuit shown in the shaded area of Fig. 7.

The *LC* bandpass filter circuit was implemented in a 0.5- μ m bipolar process for a nominal center frequency of 1 GHz. This process is a self-aligned double-polysilicon process with maximum f_t of 25 GHz and maximum f_{max} of 40 GHz for the polyemitter bipolar transistor. The inputs are buffered by emitter followers, while the outputs are buffered by a differential amplifier with a unity gain.

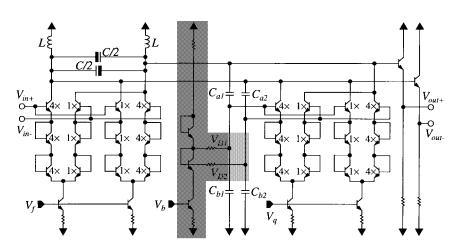


Fig. 7. Schematic of a linear active-LC filter.

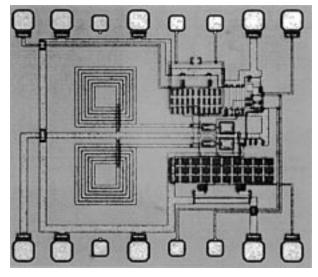


Fig. 8. Chip microphotograph of the linear active-LC filter.

Both inputs and outputs have $50-\Omega$ termination resistors to enable test on a wafer-probe station. The implemented core circuit of the test chip consumes a silicon area of 700 \times 850 μ m². Fig. 8 shows the fabricated chip microphotograph. The component values in the design are: L = 7.0 nH, C = 1.316 pF, $C_a = 1.0$ pF, and $C_b = 2.0$ pF. The chip was tested on a wafer prober through a gigahertz probe card. To test the chip differentially, a pair of two-way 180° broad-band power splitters/combiners were used to implement the single-endedto-differential and differential-to-signal-ended converters required at the input and output of the filter. The combiners/splitters exhibit almost flat response from 200 kHz to 17 GHz. The test results described below were calibrated based on measurements of the loss from the output of the signal generators or the network analyzer to the input probers (about 12 dB) and the loss from the output probers to the input of the spectrum analyzer or the network analyzer (about 12 dB). Fig. 9 shows two measured frequency responses of the filter using a network analyzer with Q tuned to 40 and 200, respectively. For a Q of 40, the filter achieved 7 dB of gain and drew 13.6 mA current in total from a 5-V supply. It was found that Q can be readily adjusted from 4 to 300 and the center frequency shift during Q tuning is small (from 994 MHz for a Q of 40 to 984 MHz for a Q of 200). If care is taken to avoid oscillation, Qcan be tuned up to 400 with the center frequency located at 983.5 MHz. The linearity of the filter was tested by performing an in-

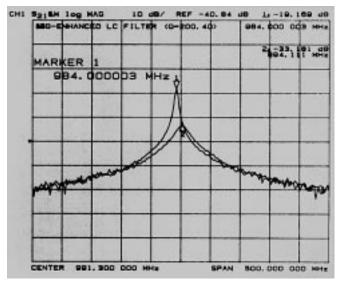


Fig. 9. Measured frequency response of the linear active-LC filter.

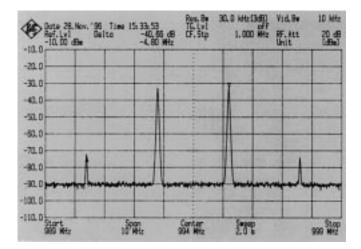


Fig. 10. Two-tone IM3 measurement of the active-LC filter.

band two-tone test for a Q of 40. Two input tones with -27 dBm signal power into the test chip were placed at $f_1 = 992.8$ MHz and $f_2 = 995.2$ MHz. They were 2.4 MHz apart within the filter passband. The third-order intermodulation products fell at 990.4 and 997.6 MHz, which were also in the filter passband. Fig. 10 shows

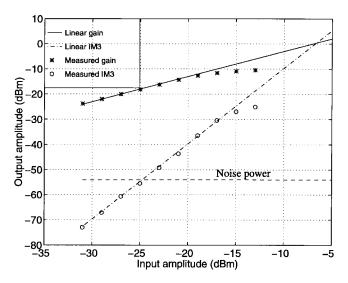


Fig. 11. Measured third-order intercept point plot.

TABLE IMeasured Performance of the Linear Active-LC Filter for Q = 40

Parameters	Experimental	Ref. [4] $(Q = 35)$
Technology	$0.5 \mu\text{m} \& 25 \text{GHz} f_t$ double-poly bipolar	0.8 µm bipolar
Chip area	700×850 μm ²	0.38 mm ²
Power supply	5 V	2.8 V
Power consumption	68 mW (13.6 mA)	24.36 mW (8.7 mA)
Q tuning range	4 ~ 400	3 ~ 350
Center frequency	994 MHz	1.825 GHz
Gain	7 dB	7 dB
Output noise density @ 994 MHz	-130 dBm/Hz (-54 dBm noise power)	-123.5 dBm/Hz (-44.5 dBm noise power)
SFDR	36 dB	30 dB
IIP3	-6.67 dBm	-23.5 dBm

the measured output spectrum from the frequency spectrum analyzer, from which it can been seen that the IM3 product power is 40.66 dB below the output signal power. The output noise power density at 994 MHz for a Q of 40 was -130 dBm/Hz. The noise bandwidth is $\Delta f = \pi f_o/2Q = 39.03$ MHz, and therefore the noise power is about -54 dBm (441.76 μ V rms). For comparison, SPICE simulation gave output noise power density of -131 dBm/Hz, and an integrated noise power of -55 dBm (394.92 μ V rms). The major contributors to the output noise of the filter are the lossy inductor itself and the feedback transconductor due to the large Q-tuning current required. Fig. 11 is the measured IP3 plot of the filter for a Q of 40. The input intercept point (IIP3) is about -6.67 dBm. The spurious-free dynamic range at this Q is about 36 dB. Table I summarizes the measured results of the test chip. This table also includes the results from [4] taking into account the external losses in the test circuitry. It can be seen that our chip has achieved significant performance improvements in IIP3 point and spurious-free dynamic range. It should be noted here that a larger dynamic range and a lower current drain can be expected for integrated active-LC filters at 2 GHz since monolithic inductors exhibit a better quality factor at this frequency.

V. CONCLUSION

A linearization method for monolithic active-LC bandpass filters was introduced in the paper. It was shown that the multi-tanh technique is appropriate for implementing the Q-enhancement transconductor. Various multi-tanh translinear circuits were discussed in terms of linearity and power dissipation. A prototype filter based on the linearization technique was fabricated in an advanced 0.5- μ m bipolar process. It was demonstrated that the Q of the filter can be tuned up to 400. For a Q of 40: the filter achieved 7-dB gain, -6.67-dBm IIP3 point, 36-dB spurious-free dynamic range; it operated at 994-MHz center frequency in measurements, while the designed nominal frequency was 1 GHz.

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