

# A Wide-Range Tunable 25MHz-110MHz BiCMOS Continuous-Time Filter

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## ABSTRACT

A high speed bandpass continuous-time biquad filter is implemented in a 0.8 $\mu\text{m}$  BiCMOS technology. It demonstrates a wide range of frequency tunability from 25MHz-110MHz. The filter intermodulation distortion stays below -52dB at 50MHz with 100mV<sub>p</sub> input differential signals. The power consumption ( $f_o = 50\text{MHz}$ ) is 90mW with a single 5V supply.

## 1. INTRODUCTION

The transconductor-capacitor (TC) or  $G_m$ - $C$  technique is a well-known approach for implementing high-speed continuous-time filters. They were commercially used quite early with bipolar technology [7]. They have been developed in different technologies such as CMOS [8], bipolar [9] and BiCMOS [5],[2],[3]. They have been chosen for many industrial applications including the read channel of disk drives [9],[2], high-speed data links [10] and digital TV and/or HDTV [3]. In this article we present a biquad bandpass filter implemented in BiCMOS technology for the realization of on-chip selectivity for radios.

## 2. TRANSCONDUCTOR-C-AMPLIFIER DEVICES

For many high-speed transconductor-C filters a simple single-stage transconductor (sometimes just an inverter structure [1]) is used. However, the DC gain of this kind of transconductor is very low and usually parasitic capacitances are high. Therefore, normally a very wide range of tuning is required to compensate the non-ideal effects such as parasitic capacitances and poor output impedances. Another class of transconductors with the general structure shown in Fig. 1 can be recognized as transconductor-Miller-integrator (TMI) or transconductor-C-amplifier (transconductor-C-opamp) [2],[3]. Basically it consists of two stages. The first stage is a conventional transconductor and the second stage is a high gain amplifier or opamp with feedback from a

Miller capacitor usually in series with a resistor (triode mode NMOS device as shown in Fig. 1). Since an "opamp" (operational amplifier) usually refers to a multiple-stage amplifier with a low-impedance output stage, the more general term "TC-amp" (for transconductor-C-amplifier) is used in this paper.

Some important features for this class of transconductors are:

i) Since the gain of second-stage amplifier is high, the voltage swing at the input of the second-stage amplifier is low (behaving as a virtual ground). Thus a very small portion of the first stage transconductor's output current flows to the parasitic capacitances connected between the amplifier inputs and ground. The low input voltage swing at the second-stage amplifier input lowers its non-linearity contribution in the entire circuit as opposed to ordinary open-loop multi-stage amplifiers in which the very last stage is responsible for producing a major non-linearity.

ii) The unity-gain frequency of a TC-amp integrator shown in Fig. 1 is given by  $2g_m/C_m$  like a single-stage transconductor (where the  $g_m$  represents the differential input transconductance). Therefore, the unity gain frequency of a TC-amp can be tuned through adjusting the input stage transconductance  $g_m$ , for example with a frequency control voltage  $V_{freq}$  as shown in Fig. 1.

iii) The entire TC-amp DC gain is the product of the DC gain of the input transconductor and the second-stage amplifier. Thus, producing a very high DC gain for a TC-amp is easier. The high DC gain with use of a feedback Miller capacitance moves the dominant pole frequency to  $\omega_o/A_{dc}$ . Creating a very low dominant pole is always desirable for making a good quality integrator. The reason is that if the second pole (and/or other parasitic poles and zeros) are located at a high frequency far from the operating frequency an almost flat  $-90^\circ$  phase and a -20 dB/decade gain frequency response in a very wide frequency range could be

achieved.

iv) The undesired excess phase of a TC-amp produced by higher parasitic poles and zeros can be compensated through adjusting the (Miller) resistors placed in series with the Miller capacitors. For example, with a voltage controlled MOSFET resistor which is tuned by a gate voltage  $V_{ph}$  as shown in Fig. 1.

v) The trade off between a TC-amp and a simple structure transconductor is speed. Of course a simpler transconductor can provide faster operation compared to a two-stage TC-amp when both are implemented in the same technology. However, as will be shown, in a  $0.8\mu\text{m}$  BiCMOS process [4] it is practical to implement a TC-amp bandpass filter over 100s of MHz range.

There is also a trade-off among noise, tunability, speed and linearity.

### 3. FILTER ARCHITECTURE

To design a second-order system (resonator), two integrators, one with positive gain and the other negative, can be connected back to back in a loop as shown in Fig. 2. Implementation of an integrator with a negative sign is performed by cross-coupling a balanced differential transconductor as shown in Fig. 2. In order to supply the input signal, a multi (two)-input transconductor has been used as shown in Fig. 2. The transconductors are tuned by  $V_{freq}$  and the overall phase of each TC-amp integrator by  $V_{ph}$ . Having assumed that the whole current of the transconductor stages shown in Fig. 2 flows into the Miller branches across the amplifier stages (the virtual ground assumption at the input of amplifiers), it can be shown that the bandpass transfer function for this second-order system is as the following:

$$\frac{V_o}{V_i} =$$

$$\frac{g_{mb}}{C_x} \cdot \frac{1}{1 + g_{mx}g_{mf}R_{ph}^2} s(1 + R_{ph}C_x s) \quad (1)$$

$$s^2 + \frac{g_{mx}g_{mf}R_{ph}}{1 + g_{mx}g_{mf}R_{ph}^2} \left( \frac{1}{C_f} + \frac{1}{C_x} \right) s + \frac{g_{mx}g_{mf}}{C_x C_f} \cdot \frac{1}{1 + g_{mx}g_{mf}R_{ph}^2}$$

where the  $g_{mb}$  represents the input transconductance and the  $g_{mf}$  and  $g_{mx}$  terms represent the loop transconductances. The NMOS transistors in the Miller branches are represented by  $R_{ph}$  i.e. a linear resistor which can be varied by  $V_{ph}$ . From (1) it can be noticed that the variation of  $R_{ph}$  changes the  $s$  coefficient in the denominator and consequently the Q of the filter. It

should be noted that the variation of the  $1/(1 + g_{mx}g_{mf}R_{ph}^2)$  term in (1) is negligible in our design: for example at 50MHz center frequency it varies between 1 to 0.96. So, the variation of Q by  $R_{ph}$  almost doesn't affect the center frequency  $f_o$ . Taking into account the exact effect of the amplifier stages with finite gain and parasitics makes (1) very complicated. However, one can simply notice that the  $V_{ph}$  voltage only adjusts the phase of each TC-amp integrator inside the loop which in turn tunes the Q of the overall filter.

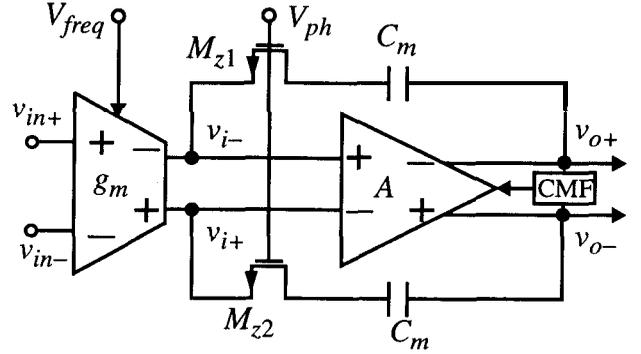


Fig. 1: Simplified schematic of a differential TC-amp integrator where  $M_{z1}$  and  $M_{z2}$  perform excess phase compensation.

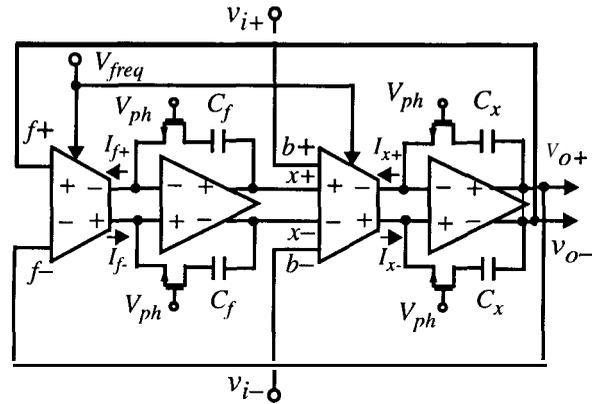


Fig. 2: A simplified second-order TC-amp based biquad loop.

## 4. CIRCUIT DESCRIPTION

### 4.1. The BiCMOS Differential Transconductor

A BiCMOS transconductor circuit, as shown in Fig. 3, has been designed to work as the input transconductor  $g_m$  of the TC-amp integrator. The cross-coupled configuration provides a very high CMRR. The HSPICE simulation shows that its common-mode gain is about -26dB (CMRR of 44dB). The inter-stage common-

mode voltage should properly be set by an additional common-mode feedback circuit, but that was not included. This level is therefore defined by the output impedance of the first stage, and may be biasing the second stage devices at the edge of saturation, increasing distortion.

The input devices i.e.  $M_1, M_2, M_{11}$  and  $M_{12}$  are NMOS transistors working in triode mode [5],[6],[2]. In other words, for these transistors  $V_{ds} \leq V_{gs} - V_{th}$  with a safe margin. The input NMOS drain-source voltage  $V_{ds}$  is in order of 100 mV and  $V_{gs}$  is biased at analog ground (2.5 V here). The drain-source voltage  $V_{ds}$  is set by the base voltage of  $Q_1, Q_2, Q_{11}$  and  $Q_{12}$  labelled  $V_{freq}$  in Fig. 3. The transconductance of an NMOS transistor in triode

can change their  $V_{ds}$  through changing the BJT  $Q_1, Q_2, Q_{11}$  and  $Q_{12}$  base voltage ( $V_{freq}$ ) and consequently change the resonance frequency.

## 4.2. The Second-Stage Amplifier

Since the two stage TC-amp integrator is insensitive to parasitics, the design of the second stage amplifier is not very crucial. However, in order to achieve high gain and high speed capability, a differential bipolar circuit with cascode PMOS load has been designed. The amplifier circuit with its continuous-time common-mode feedback circuit is shown in Fig. 4. The simulation shows that the second-stage amplifier by itself provides a DC gain greater than 57 dB, its unity-gain bandwidth is 820 MHz, its phase margin is  $77^\circ$  when driving a 2.5 pF load.

## 5. EXPERIMENTAL RESULT

Fig. 5 is a photomicrograph showing the biquad band-pass filter as part of a bigger chip. The center frequency

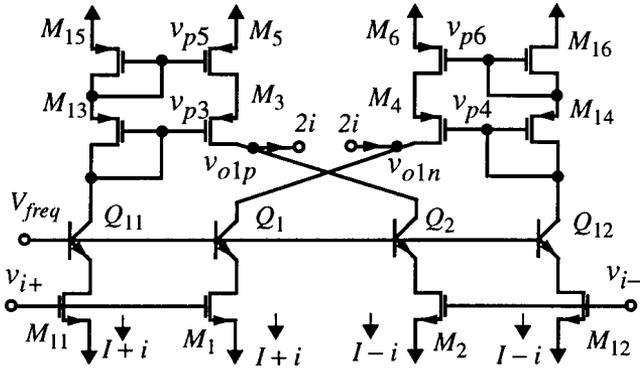


Fig. 3: The basic differential cross-coupled BiCMOS transconductor.

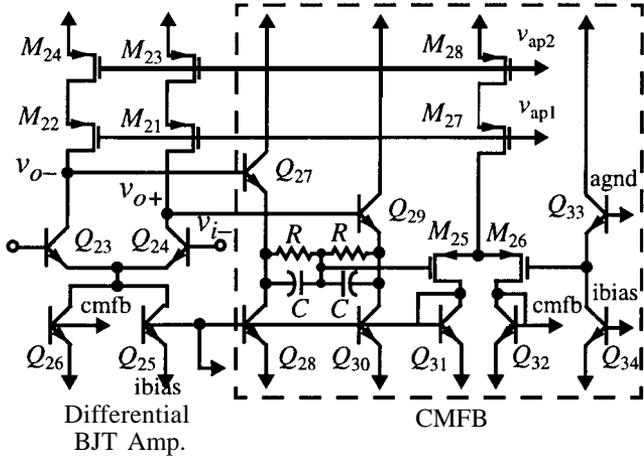


Fig. 4: Schematic diagram of the second-stage amplifier with a continuous-time CMFB circuit.

can simply be expressed by  $g_m = \mu_n C_{ox} (W/L) V_{ds}$ . So, in order to control the  $g_m$  of the input transistors one

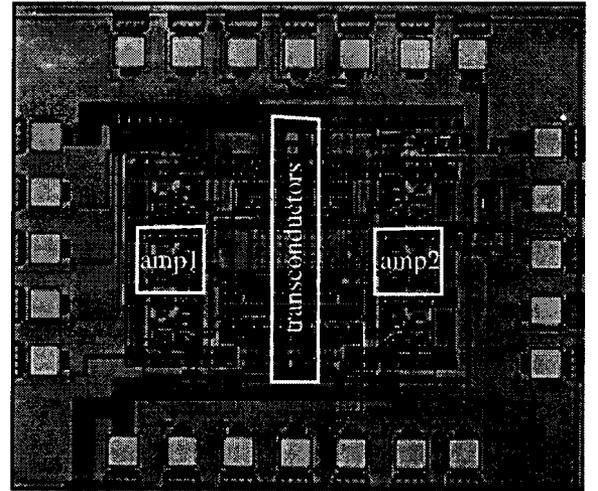


Fig. 5: Photomicrograph of the bandpass biquad fabricated as part of a bigger chip enclosed in white boundaries.

of the bandpass filter has been varied by the  $V_{freq}$  control voltage. A wide range of tuning from 25MHz to 110MHz has been achieved experimentally. Fig. 6 shows a plot of the filter's output spectrum operating at three different center frequencies. The Q of the filter was adjusted by the  $V_{ph}$  control voltage almost without changing its center frequency as expected. Fig. 7 shows a plot of the filter Q adjustment with  $f_o=50$ MHz. The other experimental results including the intermodulation linearity performance and its dynamic range are summarized in Table 1. The IM3 values given in Table 1 show the third order intermodulation levels with

respect to the total input power i.e. each tone power plus 3dB. All of the figures in Table 1 (unless mentioned) have been obtained from the measurements of the filter with Q of 3 and  $f_o=50\text{MHz}$ .

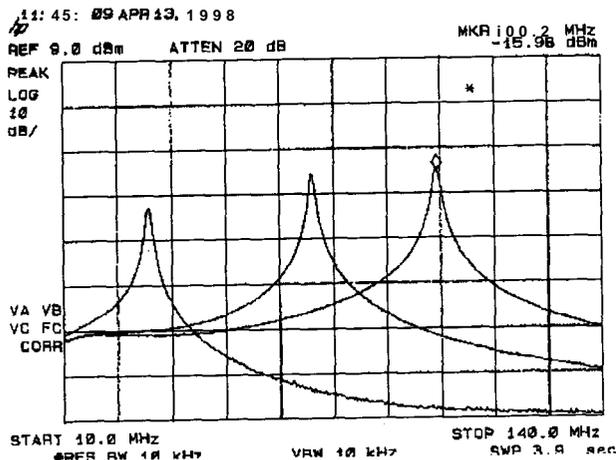


Fig. 6: The center frequency of the bandpass filter is tuned at three different frequencies: 30MHz, 70MHz and 100MHz.

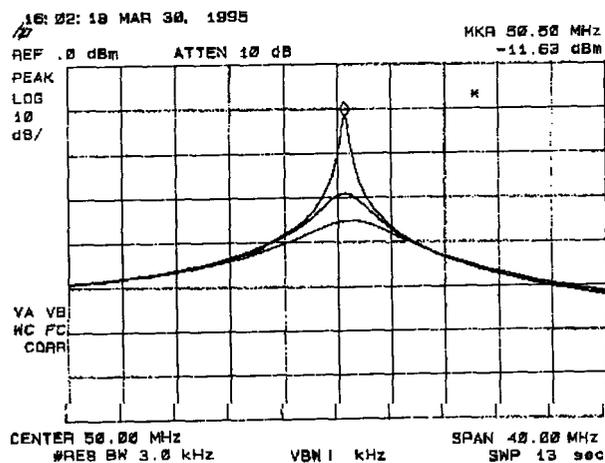


Fig. 7: Three different Q adjustments for the bandpass filter centered at 50.5MHz: Q=8, Q=18, Q=170.

## REFERENCES

[1] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 2, Feb. 1992.

[2] C. A. Laber and P. R. Gray, "A 20-MHz Sixth-Order BiCMOS Parasitic-Insensitive Continuous-Time Filter and Second-Order Equalizer Optimized for Disk-Drive Read Channels," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp. 462-470, Apr. 1993.

[3] S. D. Willingham, K. W. Martin, and A. Ganesan, "A BiCMOS Low-Distortion 8-MHz Low-Pass Filter," *IEEE J. Solid-State Circuits*, vol. 28, No. 12, pp. 1234-1245, Dec.

1993,

[4] R. Hadaway, et. al, "A Sub-micron BiCMOS Technology for Telecommunications," *J. of Microelectronic Engineering*, vol. 15, pp. 513-516, 1991.

[5] G. Groenewold, "A High-Dynamic-Range Integrated Continuous-Time Bandpass Filter," *IEEE J. Solid-State Circuits*, vol. 27, No. 11, pp. 1614-1622, Nov. 1992.

[6] R. Alini, A. Baschiroto, and R. Castello, "Tunable BiCMOS Continuous-Time Filter for High-Frequency Applications," *IEEE J. Solid-State Circuits*, vol. 27, No. 12, pp. 1905-1915, Dec. 1992.

[7] K. W. Moulding, J. R. Quartly, P. J. Rankin, R. S. Thompson, and G. A. Wilson, "Gyrator Video Filter IC with Automatic Tuning," *IEEE Journal of Solid-State Circuits*, Vol. SC-15, No. 6, pp. 963-968, Dec. 1980.

[8] V. Gopinathan, Y. P. Tsvividis, K. S. Tan, R. K. Hester, "Design considerations for high-frequency continuous-time filters and implementation of an antialiasing filter for digital video," *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 6, Dec. 1990.

[9] G. A. De Veirman and R. G. Yamasaki, "Design of a Bipolar 10-MHz Programmable Continuous-Time  $0.05^\circ$  Equiripple Linear Phase Filter," *IEEE J. SolidState Circuits*, vol. 27, No. 3, pp. 324-331, Mar. 1992.

[10] A. Shoval, W. M. Snelgrove and D. A. Johns, "Adaptive pulse-shaping filter," *IEEE Journal of Sel. Areas in Comm.*, Vol. 13, pp. 1692-1702, Dec. 1995.

Table 1: Experimental Results Obtained From The Filter at Q=3 and 50 MHz

Parameters	Measured Values
Frequency Tuning Range	25MHz-110MHz
IM3, 71mV <sub>rms</sub> at 50MHz	-52dBc
IM3, 71mV <sub>rms</sub> at 70MHz	-47dBc
Input Referred IIP3 (Intermodulation Intercept Point)	11dBm
SFDR (Spurious Free Dynamic Range)	33dB
Input referred noise	5mV <sub>rms</sub>
Peak Output Passband Noise Density (at 50MHz)	-112dBm/Hz
1 dB Compression Input Level	180mV <sub>rms</sub>
Power Dissipation	90mW
Active Area	0.35mm <sup>2</sup>