Floating Gate Charge-Sharing: a Novel Circuit for Analog Trimming

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ABSTRACT

A floating gate charge-sharing circuit that can be electrically programmed for precise positive and negative voltage changes, and can be implemented in a standard CMOS VLSI process is presented. With the advantage of its long-term charge-retention, the floating gate charge-sharing circuit is suitable for providing a compact, non-volatile and high-precision analog trimming method to trim the offset voltage resulting from unavoidable mismatches in analog circuits such as op-amps and comparators

I. INTRODUCTION

Since DC offsets seriously degrade the performance of analog integrated circuits [1][2], they should be reduced as much as possible in analog system design. DC offsets arise from process variations, temperature, and aging. Therefore there is a need to track DC offsets and their variation with high resolution.

Floating gate MOS devices are prospective analog trim-voltage storage elements for trimming the values of DC offsets [3][4]. They can be small, power-efficient, non-volatile, and electrically programmable. However, because of the steep Fowler-Nordheim tunneling I – V characteristics and the asymmetric characteristics it is not easy to control the stored charge linearly and precisely to make fine adjustments of trim voltage and/or trim current both up and down. This paper proposes a floating gate charge-sharing circuit to control the transfer of small amounts of charge onto or off the floating gate and hence obtain small trim steps.

II. THE FLOATING GATE CHARGE-SHARING CIRCUIT

A. Circuit schematic and operation principle

Recall that the floating gate is completely isolated by surrounding layers of oxide and acts as a capacitor with long-term charge retention capability [4]. A floating gate charge-sharing scheme, shown in Fig. 1, is proposed to control the transfer of a small quantity of charge. It consists of capacitors C_1 and C_2, and a tunneling switch. When the tunneling switch turns on, an amount of charge A Q will be transferred between C_1 and C_2 until the switch turns off. The quantity of transferred charge depends on the ratio of capacitors and the characteristics of the tunneling switch.

Fig. 2(a) shows a circuit implementation of the above scheme. The parasitic capacitance, C_{INJ}, loading the injection node (diffusion region) of the tunneling injector, corresponds to C_1. C_{INJ} is the sum of the diffusion capacitance of the tunneling injector, the overlapping capacitance between the floating gate and the diffusion region of the tunneling injector, and the drain or source diffusion capacitance of transistor M_R. The capacitance C_{FG} loading the floating gate corresponds to C_2. The injection of charge onto or off the floating gate is controlled by the tunneling injector through quantum tunneling. A relatively tig C_{FG} and a much smaller C_{INJ} are desired to make the source impedance high and so control the transfer of a small amount of charge. The tunneling injector is, as in [3] and [4], constructed with comers of gate polysilicon over device diffusion. Tunneling relies on field enhancement at the comers.

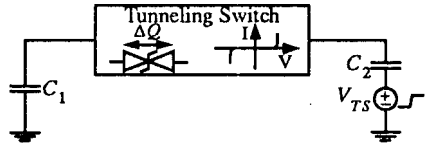

Fig. 1. The conceptual diagram of the floating gate charge-sharing.

The floating gate charge-sharing circuit has two modes of operation: TRIM mode and READ mode. In the TRIM mode, charge transfer occurs between the floating gate and the injection node of the tunneling injector; the voltage on the floating gate is updated by a small step AV_{FG}. In the READ mode, the floating gate voltage is held at its latest updated level and is read via the sense transistor M_S. Fig. 2(b) illustrates the operation waveforms.

TRIM is performed by using the tunneling injector to inject charge onto or remove it from the floating gate. Tunneling takes a very short time [6]. When a positive programming voltage is applied to the control gate, electrons are injected onto the floating gate from the injection node of the tunneling injector, and so the floating gate voltage V_{FG} is decreased and the injection node voltage V_{INJ} is increased. Similarly when a negative programming voltage is applied, electrons are removed from the floating gate and henceforth V_{FG} is increased and V_{INJ} is decreased. The exponential tunneling current results in a charge sharing between the relatively large capacitance C_{FG} and the much smaller

capacitance C_{INJ}. When the magnitude of the voltage across the tunneling barrier, $|V_{FG} - V_{INJ}|$, drops to the absolute value of tunneling field emission threshold V_{FE} (forward) or V_{RE} (reverse), the tunneling process is stopped and no more charge will be transferred (the tunneling injector operates like a switch). Therefore, a very small change in the floating gate voltage, A V_{FG}, is achieved in each TRIM operation. ΔV_{FG} *is* mainly determined by the capacitive ratio C_{FG}/C_{INJ}, *the* programming voltage V_{PH} or V_{PL}, and the memorized voltage on the floating gate.

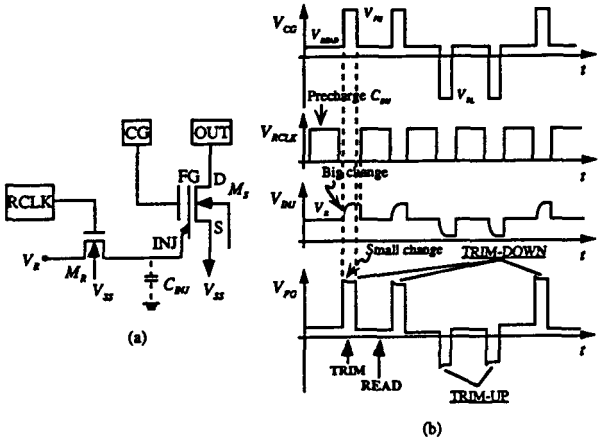

Fig. 2. A floating gate charge-sharing circuit (a) circuit schematic; (b) operation timing diagram.

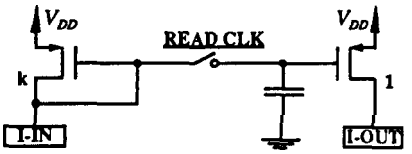

Fig. 3. A dynamic current-in current-out circuit with the scaling ratio of k.

READ mode is used to hold the latest trim-voltage level and read it from the OUT node as a buffered current for trimming. A fixed voltage V_{READ} is applied to the control gate for this purpose. The parasitic capacitance C_{INJ} is precharged to the RESET voltage V_R during READ, during which the floating gate capacitance C_{FG} retains its charge. It has been demonstrated in the literature that the charge loss of the floating gate device is less than 0.1 percent over a ten year period at temperatures below $100°C$ [3]. Therefore, the charge drift during READ is negligible, i.e., the updated trim voltage/current levels can be kept for a sufficiently long time for practical applications. An output current, depending on the updated trim voltage V_{FG} *(READ)* and the drain voltage of the sense transistor V_{DS}, *can be* drawn from the drain of the sense transistor M_S. The READ current *can be used* to add (or reduce) an amount of current to one side of a differential pair comparator or op-amp and in so doing compensate for DC offsets. This can be achieved (for example) via a dynamic analog current-in current-out circuit shown in Fig. 3, which employs a sampled current mirror to isolate the drain current in TRIM. The current-in current-out circuit also provides a way to further scale down the above drain current by scaling the size between the two transistors.

B. *HSPICE simulation*

Available SPICE elements, including the Fowler-Nordheim tunneling diode, the PN junction diode, the MOSFET transistor, and capacitors, were used to model the floating gate MOS device. Basic parameters chosen for the Fowler-Nordheim tunneling diode fit our measured tunneling characteristic of the implemented tunneling injector [7]. To perform HSPICE simulations, a load resistance of $100k\Omega$ was connected from OUT to V_{DD} *to* establish a drain current. A series of programming pulses, alternating groups of positive and negative pulses with duty cycle of 5% and a period of 2ms, were applied to the control gate. The positive programmmg voltage V_{PH} and the negative programming voltage V_{PL} were 18V and -1 5.8 *V*, respectively. The RCLK clock rate was 500Hz. The simulated circuit had V_R=2.5V, V_{FE}=12V, V_{RE}=−15V, V_{DD}=5V, V_{SS}=0V, and C_{FG}/C_{INJ}=100.

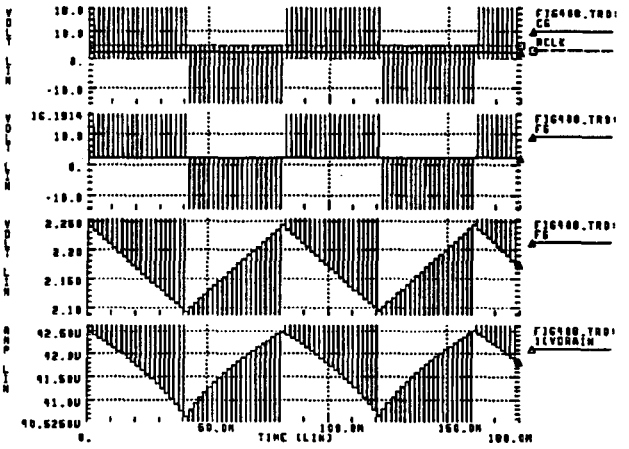

Fig. 4. HSPICE simulation for the operation waveforms of the floating gate charge-sharing circuit: (a) RESET clock and programming pulse train; (b) floating gate voltage; (c) updating voltage levels on the floating gate during READ; (d) updating drain current levels of the sense transistor during READ.

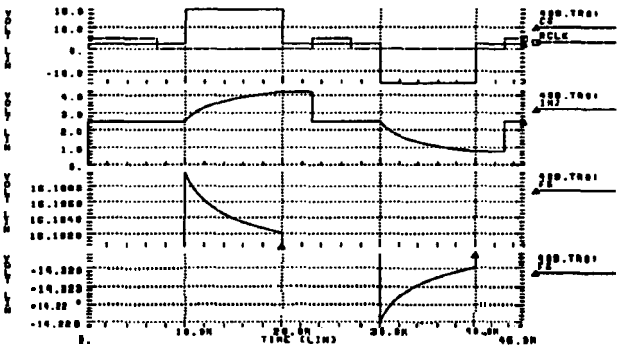

Fig. 5. HSPICE simulation for the charge-transfer characteristics of the floating gate charge-sharing circuit during TRIM: (a) RESET clock and programming pulses; (b) the variation in V_{INJ}; *(c) the* variation in V_{FG} in positive programming direction: (d) the variation in V_{FG} in negative programming direction.

The simulated waveforms are shown in Fig. 4, which conform with the analysis given in subsection A. It can be seen that the resulting step size is not the same in each pulse operation, but changes slowly versus the number of pulse in each direction. We can also see that trim-voltage/trim-current levels are retained well and that achieved step sizes are very small ($\leq 7.5mV$). A slower programming rate was also used in our simulation, which resulted in almost the same operation waveforms.

Fig. 5 shows the simulated results for the charge-transfer process during TRIM. As expected the change in V_{INJ} (1.6576V) is much larger than the change in V_{FG} (0.0075V).

C. ***Trimming step size modelling***

During the TRIM operation, the charge transferred between the floating gate and the injection electrode of the tunneling injector is: $\Delta Q(n)=C_{INJ}|\Delta V_{INJ}(n)|=C_{FG}|\Delta V_{FG}(n)|$. Based on this and a capacitive coupling model of the floating gate device [4], we can obtain the following equations [7]

$$\Delta V_{FG}(n) = \frac{C_{INJ}}{(1-P_F)C_{INJ}+(1-P_I)C_{FG}} \cdot \cdot[(1-P_IP_F)V_{FE}+(1-P_I)V_R - -(1-P_F)(P_{CG}V_{PH}+V_{FG}(n-1)-V_{FG}(0))] \quad (1)$$

expresses the trimming step size due to the injection of electrons onto the floating gate, and

$$\Delta V_{FG}(n) = \frac{C_{INJ}}{(1-P_F)C_{INJ}+(1-P_I)C_{FG}} \cdot \cdot[(1-P_IP_F)V_{RE}+(1-P_I)V_R - -(1-P_F)(P_{CG}V_{PL}+V_{FG}(0)-V_{FG}(n-1))] \quad (2)$$

gives the trimming step size due to the removal of electrons from the floating gate. A note here is that: $P_{CG}=C_{CG}/C_{FG}$, $P_I=C_{FI}/C_{FG}$, and $P_F=C_{FI}/C_{INJ}$, where C_{FI} is the capacitance between the floating gate and the injection electrode of the tunneling injector. In the design of the floating gate charge-sharing circuit, a very small C_{FI} is desired to reduce the value of C_{INJ} and the coupling from the floating gate to the injection node. The coupling ratio P_{CG} is dominant in all coupling from adjacent nodes to the floating gate. P_I and P_F ***are*** hence negligible, and $V_{FG}(0)=P_{CG}V_{READ}$. From Eqs. (1) and (2) it can be seen that the floating gate charge-sharing trimming circuit has nonlinear trim-up/trim-down characteristics. The trimming step size, $\Delta V_{FG}(n)$, is mainly determined by V_{PH}, V_{PL}, and the capacitor ratio C_{FG}/C_{INJ}; larger C_{FG}/C_{INJ} and/or lower programming voltages result in smaller step sizes (better trim resolution). The limit that $V_{FG}(READ)$ attains defines a maximum trim adjustment range: $[P_{CG}V_{READ}-(P_{CG}V_{PH}-V_{FE}-V_R),\ P_{CG}V_{READ}-(P_{CG}V_{PL}-P_{CG}V_{RE}-V_R)]$. As $V_{FG}(READ)$ approaches limiting levels, the step size becomes steadily smaller. It is desired that large trim range can be achieved so that large offset voltages can be adjusted. However, this intention conflicts the requirement of trimming resolution. A larger programming voltage translates to a larger trim range but with worse trim resolution.

D. Monolithic implementation

Based on a previous attempt to use the gate oxide with corners for tunneling in a 2μm CMOS process [3], we successfully fabricated tunneling injectors using a 1.2μm n-well CMOS process [4]. The floating gate charge-sharing circuit can thus be designed in this 1.2μm CMOS process.

As stated earlier, it is desired to have the ratio of C_{INJ}/C_{FG} as small as possible. Therefore, the transistor M_R and the tunneling injector are designed using the smallest device size to achieve the smallest C_{INJ}, and a big overlap between the control gate and the floating gate is used to achieve a large C_{CG} and hence a large C_{FG}. The sense transistor we used was a small n-channel MOS transistor with equal value of width and length. To reduce the amplitude of the programming voltages, the coupling ratio P_{CG} should be designed to approach 1. This can be achieved by reducing C_{FB} (the overlap capacitance between the floating gate and the substrate). Thus, the most part of the floating gate was used to overlap the field oxide.

III. FEEDBACK-BASED TRIMMING ALGORITHM

The operation of the floating gate charge-sharing circuit needs a control circuitry to provide both positive and negative programming voltages to inject charge onto or remove charge from the floating gate. An efficient programming strategy is to embed the circuit into a feedback loop [5], which consists of an UP/DOWN counter, digital logic circuits, and high-voltage driving circuitry. The local feedback circuitry measures the extent of the uncompensated offset in the system and then decides whether trimming is needed, as well as which type of programming pulse (positive or negative) is required. Accordingly, the amount of charge on the floating gate is increased or decreased to make the floating gate voltage in READ to achieve a target value that is used to cancel the offset of the uncompensated circuit.

Because of the variability in step sizes, an iterative algorithm for updating the trim voltage/current levels to a target trim value is created by the use of this feedback loop: if the target value is not reached, more pulses of the same polarity are generated; when the target value is reached, the programming operation is stopped; if the target value is surpassed, the polarity of the programming is reversed. This feedback trimming algorithm also hints an adaptive characteristic: the variation of the offset voltage can be tracked since the programming of the floating gate charge-sharing circuit is controlled by the feedback loop, and henceforth a stable (both temperature and time) analog trimming is achieved.

Fig. 6 is an offset trimming simulation result based on the floating gate trimming algorithm, which shows that the target trim voltage (V_{TG}) are reached with a trim resolution of

O.lmV (i.e., $\Delta V_{FG}(READ)$=0.1mV). The critical parameters we chose are: C_{FG}=1pF, C_{INJ}=5μF, P_{CG}=0.9, V_{RE}=−15V, V_{FE}=12V, V_R=2.5V, and V_{READ}=2.5V. The programming voltages were selected as V_{PH}=18V and V_{PL}=−16V. The resulted adjustment range is [0.55V, 4.15V]. It was assumed that no charge is stored on the floating gate initially, and the target trim voltage is a varied value as shown in the dotted curve. It can been further demonstrated that the offset adjustment capability is relaxed with the variation of C_{FG}/C_{INJ}, and the error of V_{PH} or V_{PL} [7].

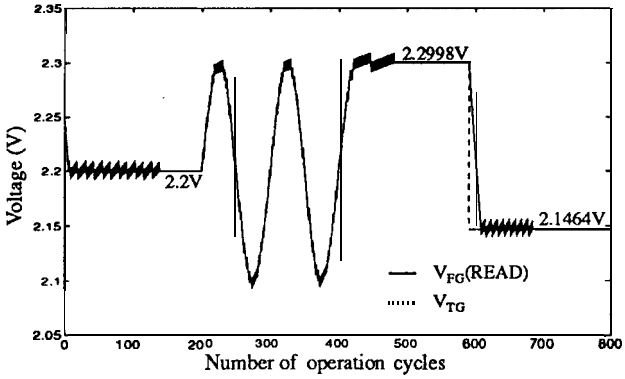

Fig. 6. An offset voltage tracking simulation.

IV. AN OFFSET-TRIMMED COMPARATOR

Fig. 7 shows a comparator front-end that employs a trim-current input: in this case, to trim the input offset voltage of a comparator, the floating gate charge-sharing circuit was configured to add or reduce an amount of current to one side of the differential input pair and in so doing compensate for DC offsets.

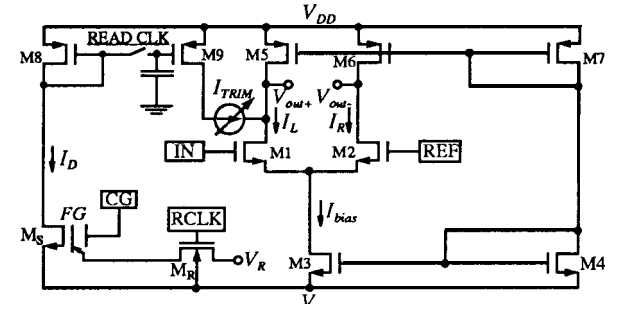

Fig. 7. A comparator front-end incorporating the floating gate charge-sharing trim memory.

The condition, $I_L = I_R$ for $V_{IN} = V_{REF}$, defines the desired switching point between the "trim-up" operation and the "trim-down" operation. If we assume the DC offset voltage of the comparator is ***Vos,*** then the target trim voltage that produce zero input offset with respect to the normal comparator inputs is

$$V_{TG} = k\left(\frac{g_m}{g_{FG}}\right) V_{OS} \qquad (3)$$

where k is the scaling ratio between M8 and M9, g_m is the transconductance of the input pair transistors (Ml and M2), and g_{FG} is the transconductance of M_S.

We have demonstrated that, in Section III, the target trim voltage V_{TG} ***can be*** approached with a resolution of O.lmV by designing the floating gate charge-sharing circuit which occupies the chip area equivalent to about 1pF capacitor. Therefore, the offset voltage of the cymparator can be improved to less than 0.1 mV by making $\frac{}{k}$ (g&g,,,) ≤ 1.

V. CONCLUSION

The proposed floating gate charge-sharing circuit does not involve many transistors but is very usable as a trim-voltage analog memory. The incorporation of the circuit into a feedback loop provides an on-line analog trimming technique to shape DC offsets, and the simulation results showed that the offset voltage in a simple comparator can be readily reduced to less than O.lmV. The successful implementation of tunneling injectors with a number of comers demonstrates that it can be implemented in a standard CMOS VLSI process.

The floating gate charge-sharing circuit is designed to be charged/discharged more than once. Its endurance performance would have to be investigated before commercial exploration of the technique.

ACKNOWLEDGMENTS

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