A 5-GHz SiGe HBT Return-to-Zero Comparator

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ABSTRACT A monolithic comparator implemented in a SiGe HBT technology is presented. The circuit employs a resettable slave stage, which was carefully designed to produce return-to-zero output data. Operation with sampling rates up to 5GHz has been demonstrated. The comparator chip has an input range of **1.5V,** dissipates 89mW from a 3-volt supply, and occupies a die area of $407\times143\mu m^2$.

Introduction

There is a demand for high-speed bandpass delta-sigma analog-to-digital converters for high-speed telecommunications systems such as satellite telephony and digital radios [l]. In high-speed A/D converters, the comparator has a crucial influence on the overall performance, especially on the speed performance, that can be achieved. Figure 1 shows a practical architecture for an LC bandpass delta-sigma A/D converter, where the comparator acts as a data sampler and one-bit quantizer. The comparator is required to produce return-to-zero (RZ) data in the feedback loop for good linearity [2].

The recently demonstrated integrated inductor [3] should, in principle, permit bandpass conversion at giga-hertz frequencies with LC resonators. This would allow digital radios to be implemented with fully monolithic digital IF and baseband stages, which requires that comparators can be sampled at 3.6GHz for a 9OOMHz carrier. GaAs has traditionally been the only contender for applications above this frequency [4]. The emergence of production ready SiGe heterojuction bipolar transistors (SiGe HBT's) offers an alternative technology which meets such high speed challenges [5]. In this paper, we report a SiGe HBT ECL return-to-zero comparator that exploits the attributes of SiGe HBT technology and achieves a sampling rate up to 5GHz.

SiGe HBT Technology

The SiGe HBT technology provided by IBM is a high performance bipolar process using a SiGe epitaxial graded-base transistor, which has a 0.5μm emitter width [6]. It features HBT NPN transistors, polysilicon resistors, three levels of metal interconnect, and substrate contacts. Typical standard device parameters for 0.5 x 2.5um (TX1) and 0.5 x 10um (TX6) emitter-are adevices are given in Table 1.

Table 1: Typical SiGe HBT Device Parameters

Parameters	TX1	TX6
$\beta\,(V_{CE} = 1V, I_C = 1mA)$	100	130
$f_T\,(V_{CE} = 1V, I_C = 1mA)$	39GHz	43GHz
$f_{MAX}\,(V_{CE} = 1\,V, I_C = 1mA)$	52GHz	5OGHz
$R_B\,(\Omega)$	195	70
C_{JE} (fF)	9.65	32.30
C_{JC} (fF)	6.10	17.42
C_{JS} (fF)	5.27	8.80
τ_F (ps)	2.64	2.67

Circuit Design

Conventional circuit configurations were used in the circuit design. The comparator circuit shown in Figure 2 consists of an input buffer, a clock buffer, a preamplifier stage, a core latching comparator, a slave latch, and an output buffer. The use of differential signals in both the data and clock paths leads to a fully symmetric topology.

The latching comparator is a conventional series gated configuration. The circuit alternates between

two operation modes: the sampling mode and the latching mode, depending on the state of the clock inputs. Clock signals, **clk** and $\overline{\textbf{clk}}$, drive the differential pair formed by Q_5 and Q_6, and steer current between two cascoded differential circuits (Q_1 to Q_4) with shared collector resistors. In the sampling mode, the latching comparator operates as an amplifier by producing the output voltage, $A_L(V_{in+} - V_{in-})$, based on the differential pair Q_1 and Q_2. In the latching mode, the other differential pair Q_3 and Q_4 is activated by the change in the state of clocking signal, and thereafter the output voltage is regenerately amplified and latched by positive feedback through emitter followers Q_7 and Q_8. The value of load resistors R_1 and R_2 can be calculated based on the output voltage swing and the bias current. However, this simple calculation may not result in an optimum value for approaching the minimum propagation delay. In the design, the bias current was selected as 1.2mA to make switching transistors operate at a point corresponding to almost the maximum device f_T over the desired range of operating conditions. A typical logic swing of custom ECL circuits is 400mV. It is, however, desirable to reduce the output voltage swing for speed and to be compatible with a 3V supply. The minimum output voltage swing is mainly limited by the voltage required to fully switch the current through the differential pair, the extrinsic emitter resistance, and the noise margin. HSPICE simulation was used in the work to draw the optimum load resistance for achieving the minimum propagation delay versus the voltage swing. Based on the simulation and the limitation on the minimum voltage swing, an internal differential logic swing was chosen as 2OOmV which resulted in load resistor values of 85Ω.

The broadband differential preamplifier stage amplifies the input signal by a gain A_P and feeds this signal into the latching comparator. This helps the output of the latching comparator change state quickly since the output swing of the latching comparator is increased to $A_P A_L(V_{in+} - V_{in-})$ in the sampling mode. To optimize the input signal response, the preamplifier was designed to have the same time constant as that of the latching comparator. To realize this, the resistor value of R_{p1} and R_{p2} was chosen as 300Ω, which sets the gain of the preamplifier to about 6.4. The emitter followers Q_{p3} and Q_{p4} were used to reduce the clock flashback to the input and make a voltage level shift. It is expected that the small base resistance of SiGe HBT's would minimize the ringing caused by fast clock steering operation. The reason is that the output inductance of the emitter follower is directly proportional to the base resistance of the emitter follower circuit [3]. This, in turn, makes the resonance between the follower load capacitance and output inductance shift to a higher frequency (about 11.7GHz based on the theoretical calculation and HSPICE simulation).

The differential output of the core latching comparator is fed to the slave stage, which is similar to the core latching comparator. To produce return-to-zero data at its output, the latching comparator used for implementing the slave stage was modified by adding a transistor Q_{r1} controlled by $\overline{\textbf{clk}}$ to asynchronously reset the latch output to the logical "0" state when the latch is in the latched logical "1" mode. Q_{r2} was added to keep symmetric differential operation. For proper return-to-zero operation, the DC voltage level of Q_{r1} has to be compatible with the output of the slave stage. However, the DC bias voltage level for the clock steering differential pairs (Q_5 and Q_6, and Q_{14} and Q_{15}) needs to be carefully set up to avoid differential pair transistors operating in saturation, especially for a 3V power supply. Voltage dividers (formed by R_{c1} and R_{c2}, and R_{c3} and R_{c4}) were therefore used to provide a proper DC bias voltage level. The slave stage also helps to reduce metastable states by providing additional amplification of the input differential signal, and it extends conversion speed by holding a stable comparison result for a complete clock cycle. A note here is that there is no sampling clock delay produced at the output of the comparator. Another master-slave stage can be added to the comparator to create one clock delay to meet the requirement of the feedback loop design of LC bandpass delta-sigma A/D converters, which would also result in further reduction of metastable effects.

The output buffer amplifiers were designed for a gain of 1 x into differential 50 ohm loads, with minimum loading of the internal comparator output, and sufficient bandwidth to minimize waveform distortion.

Standard transistors were used throughout the

comparator design. The TX1 transistor was used in the comparator design excluding the output buffer stage to minimize the power dissipation and layout area. The transistors used in the buffer circuit were TX6. The designed comparator chip contains 43 NPN transistors and 24 resistors.

Simulated and Experimental Results

The comparator has been fabricated as a part of a test chip in the IBM SiGe HBT technology. Figure 3 shows a photomicrograph of the circuit. The total test chip area is $1162\times606\mu m^2$, while the core circuit occupies an area of $407\times143\mu m^2$.

Table 2: Simulated and Measured Parameters

Parameters	Simulation	Experimental
Power Consumption	85.93mW	89.04mW
Off set Voltage	<1mV	<1mV
Input Voltage Range	1.5V	1.5V
Rise Time (l0%-90%)	62ps	avg. 76ps
Fall Time (90%-10%)	7ops	avg. 84ps
Clock Frequency	max. 5GHz	max. 5GHz
Output Voltage Swing	200mV	147mV
Sensitivity	<2mV	<4mV

Table 2 lists the simulated and experimental results for the circuit. The measured and simulation results are in good agreement. The low voltage output swing is due to manufacturing variation in nominal resistor values, which are smaller than the designed values. The return-to-zero operation of the comparator results in the difference between the rise time and the fall time in both measurement and simulation. "Sensitivity" estimates the width of the metastability region on the input when clocked at 4GHz.

Figure 4 shows simulated waveforms, while the measured input and output waveforms are given in Figure 5. Both cases were run at a clock frequency of 4GHz with the input frequency set at 1 GHz.

To demonstrate its application for A/D converters, Figure 6 shows a simulated output spectrum of the comparator embedded in a fourth-order LC bandpass $\Delta\Sigma$ modulator with centre frequency of 1 GHz and sampling frequency of 4GHz. The resultant signal-to-noise ratio for 1 OMHz bandwidth is 49.5.

Conclusion

A high-speed SiGe HBT comparator has been developed which provides good performance with sampling frequency up to 5-GHz. The giga-hertz return-to-zero data output of the comparator would make LC bandpass delta-sigma analog-to-digital conversion on silicon possible.

Acknowledgments

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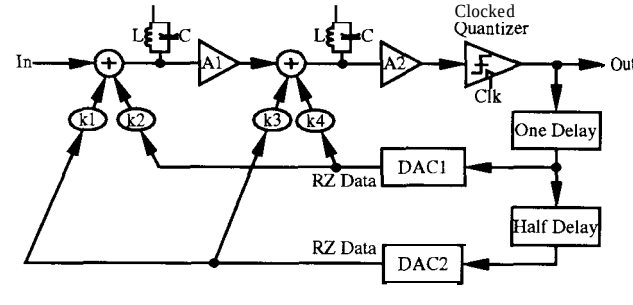

Figure!. A structure for LC bandpass AZ modulators.

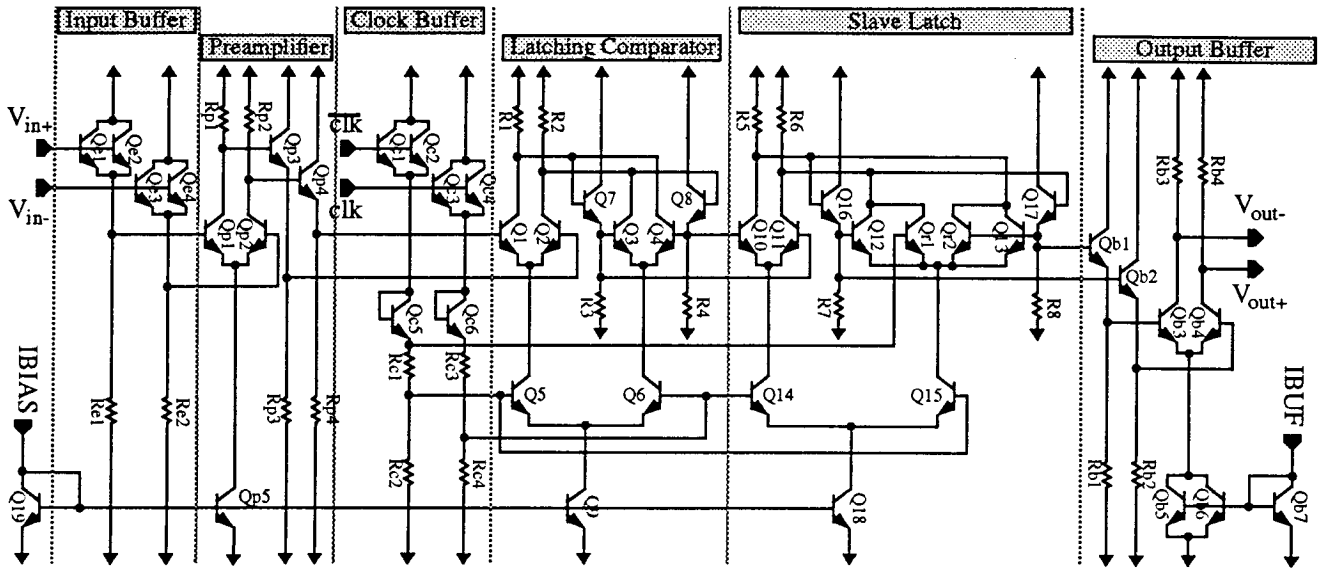

Figure 2. A complete schematic of the SiGe HBT return-to-zero comparator.

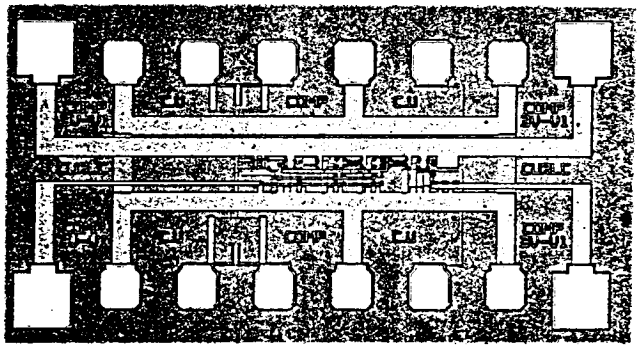

Figure 3. Chip photograph of the SiGe HBT comparator.

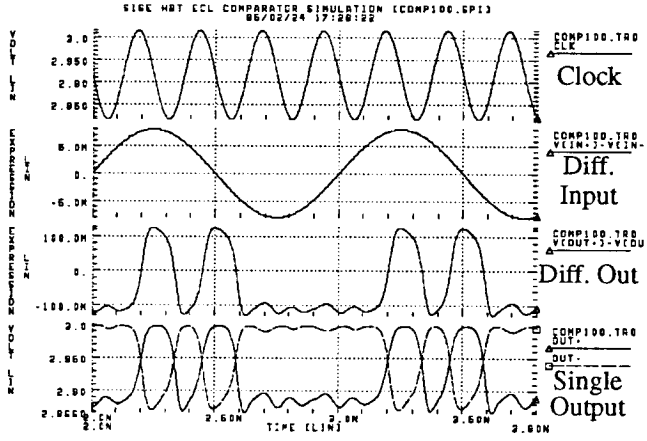

Figure 4. HSPICE simulated waveforms for the SiGe HBT comparator with sinusoid inputs.

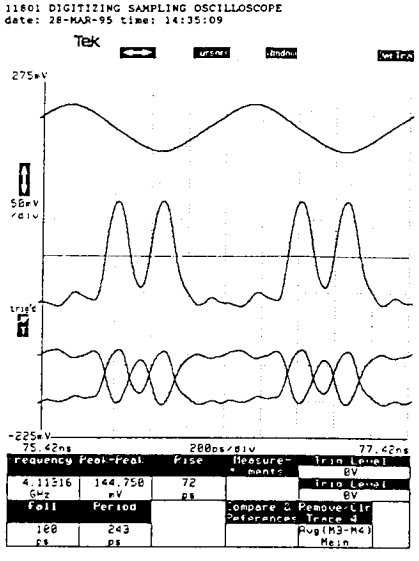

Figure 5. Measured waveforms of the SiGe HBT comparator.

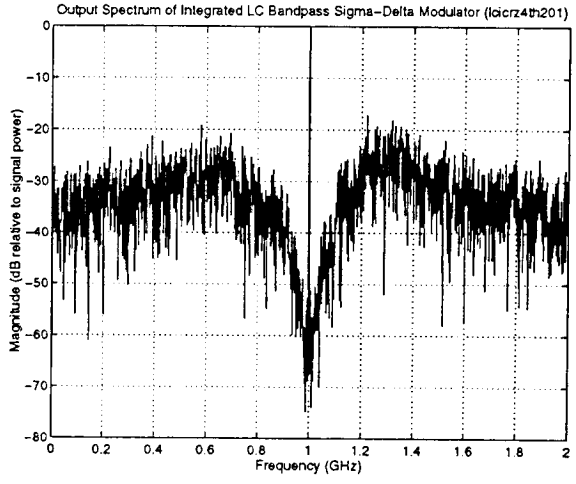

Figure 6. Output spectrum of a fourth-order LC bandpass $\Delta\Sigma$ modulator.